

**COMPAL  
CONFIDENTIAL**

**MODEL NAME : AAPB0**

**PCB NO : LA-C551P**

**BOM P/N : 4319X331L01**

**GPIO MAP: Gen7 GPIO Master\_0520**

# MIRAMAR17

**Skylake H-type (2 chip)**

**REV : 1.0 (A00)**

**2015.08.18**

**@ : Nopop Component**

**EMC@ : EMI/ESD/RF part**

**CONN@ : Connector Component**

**XDP@ : Total debug Component (pop them until ST)**

**TB@ : Thunderbolt function**

Layout Dell logo



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REV: X00  
PWB: XXXXX  
DATE: 1403-06

PCB 178 LA-XXXXP REV0 MB

Part Number	Description
DA00000000X	PCB 178 LA-XXXXP REV0 MB

Power CKT:  
0108

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**Cover Sheet**

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## POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

## PM TABLE

State	power plane	+PWR_SRC +5V_ALW +3.3V_ALW +3.3V_ALW2 +3.3V_ALW_DSW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.8V_ALW +1.0V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +3.3V_MXM +5V_MXM +MXM_PWR_SRC	+3.3V_M	(M-OFF) +3.3V_M +VCC_CORE +VCC_EDRAM +VCC_EOPIO +VCC_GTU +VCC_GT +1.0V_VCCSTG +VCC_SA
S0	ON	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	2280 SSD
SATA 1	Dock
SATA 2	
SATA 3	SATAe HDD
SATA 4	2280 SSD
SATA 5	

## Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
1	Top	3.7	Copper foil	0.5oz
2	GND/PWR	3.7	Prepreg	1050
3	Sig 1	4.1	Copper foil	1oz
4	GND/PWR	3.7	Prepreg	2116Mx2
5	Sig 2	3.7	Copper foil	1oz
6	Sig 3	3.7	Prepreg	1050Hx2
7	GND/PWR	4.1	Copper foil	1oz
8	Sig 4	3.7	Prepreg	2116Mx2
9	GND/PWR	3.7	Copper foil	1oz
10	Bottom	3.7	Prepreg	1050
			SolderMask	0.5oz
Overall Thickness (1.45mm ± 10%)				57.09

USB3.0	DESTINATION
Port 1	Left Side JUSB1
Port 2	M.2 Slot-2 (WWAN/LTE/HCA)
Port 3	Right Side JUSB1
Port 4	Right Side JUSB2
Port 5	Right Side JUSB3
Port 6	Docking

USB PORT#	DESTINATION
1	Left Side JUSB1
2	Right Side JUSB1
3	Right Side JUSB2
4	Right Side JUSB3
5	Docking USB3.0
6	M.2 Slot-1 (WLAN/BT/WiGig)
7	Docking USB 2.0
8	M.2 Slot-2 (WWAN/LTE/HCA)
9	NA
10	USH
11	Camera
12	NA
13	NA
14	NA

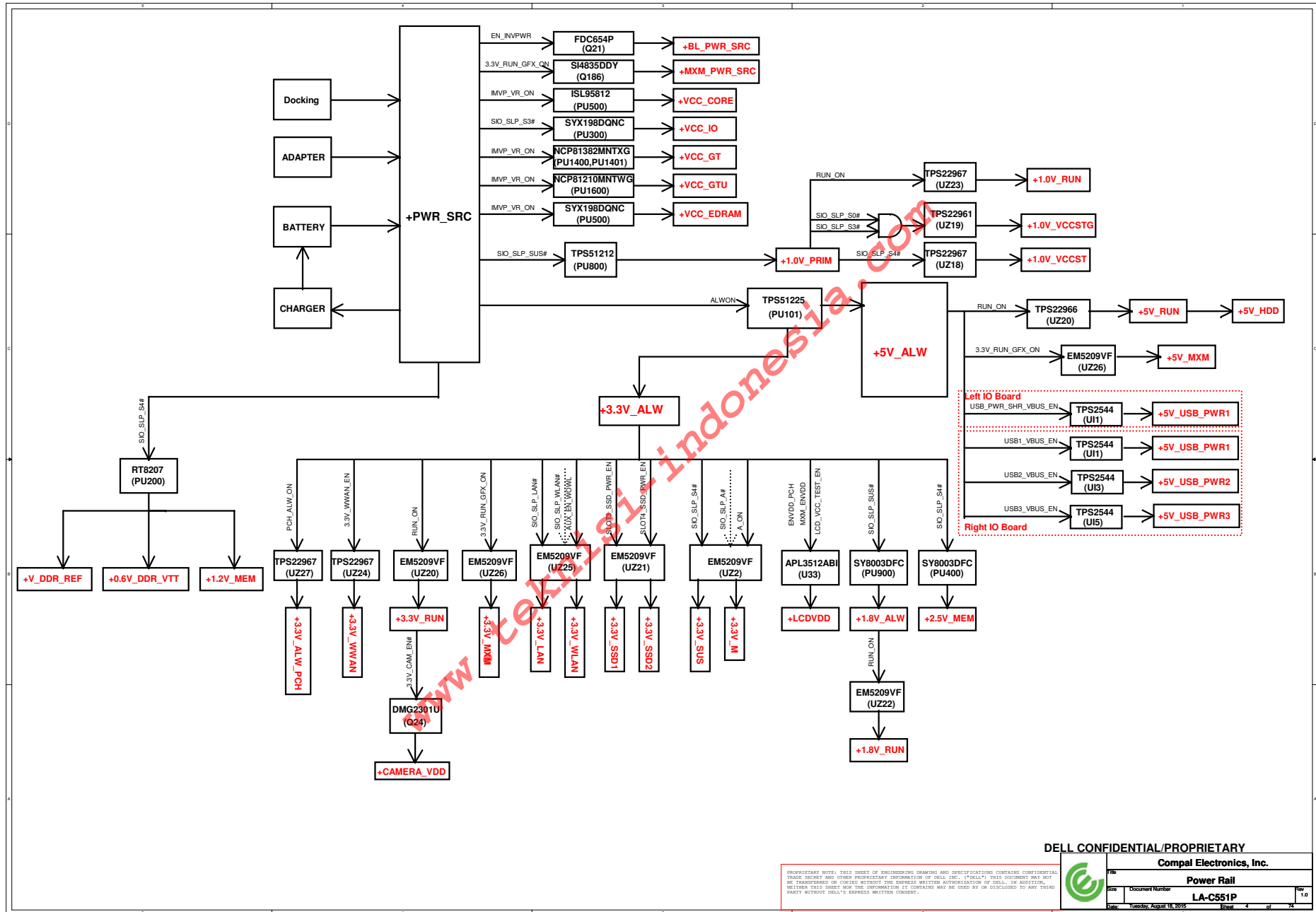
USH		
0		BIO
1		NA

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	M.2 Slot-1 (WLAN/Wigig)
Lane 3	MMI(Card reader)
Lane 4	10/100/1G LOM
Lane 5~8	TBT-Alpine Ridge
Lane 9~12	SSD 2280
Lane 13	M.2 Slot-2 (WWAN/LTE/HCA)
Lane 15~16	HDD SATA-Express
Lane 17~20	SSD 2280

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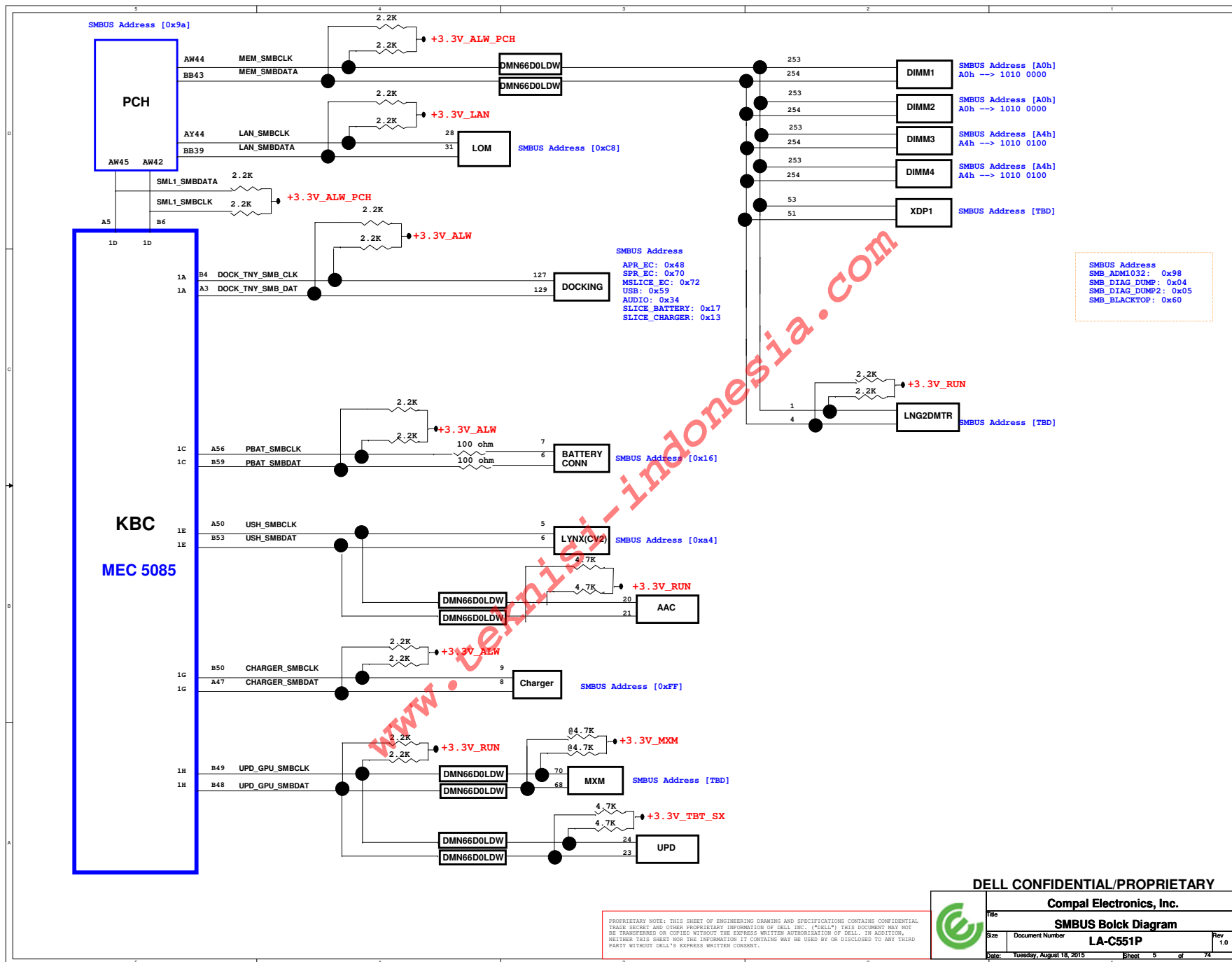
Power Rail

LA-C551P



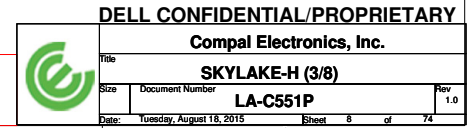
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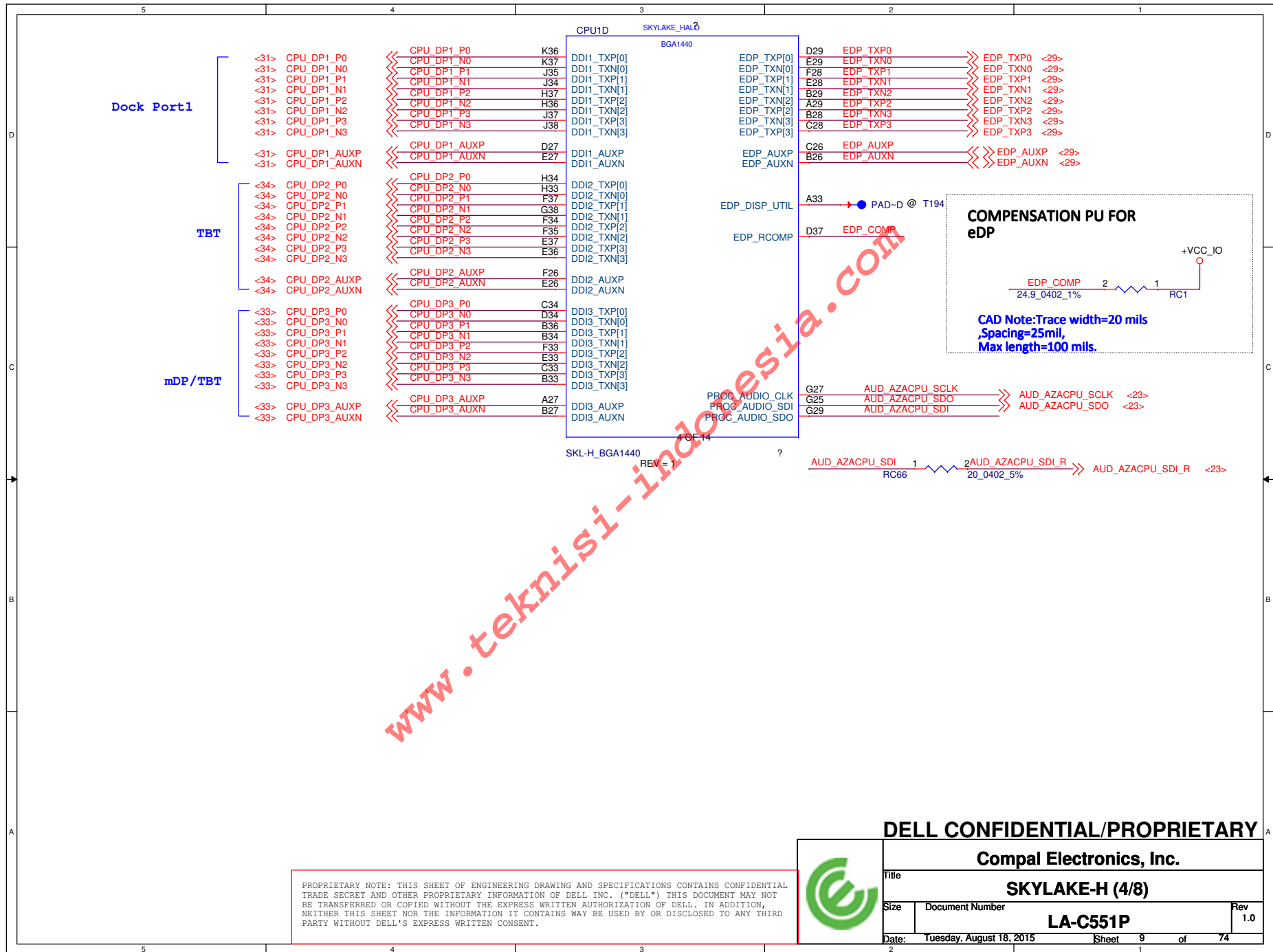


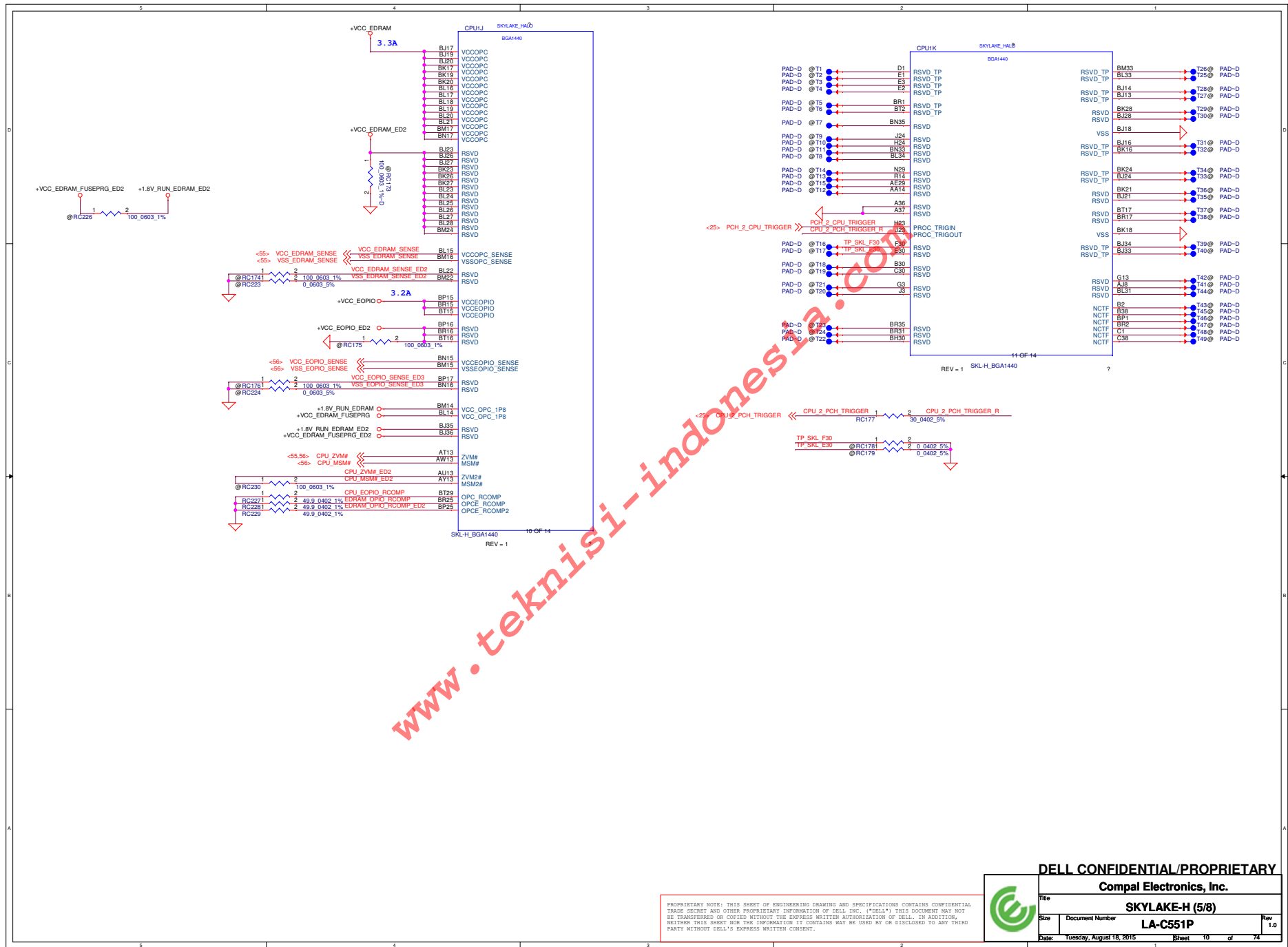




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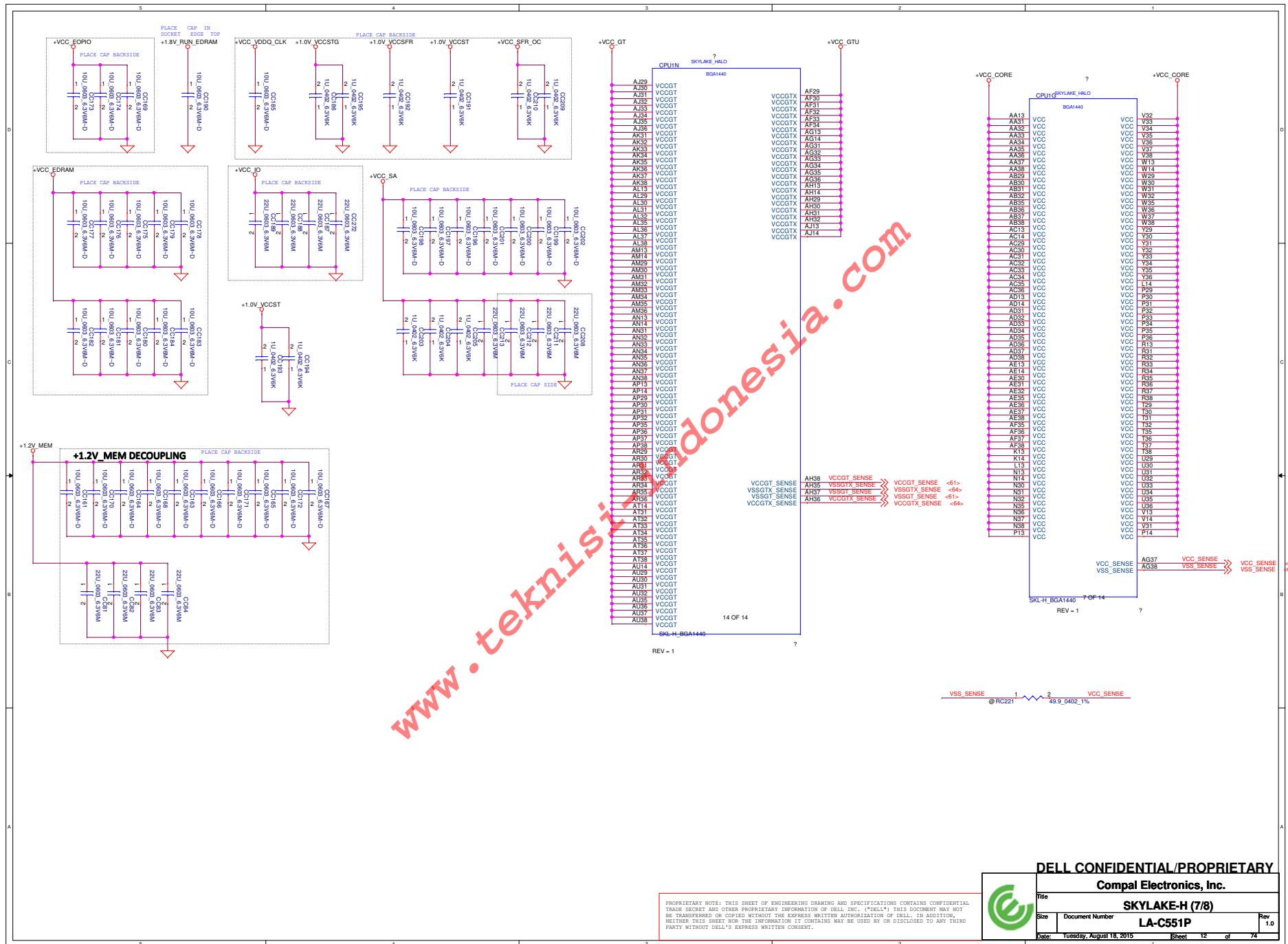


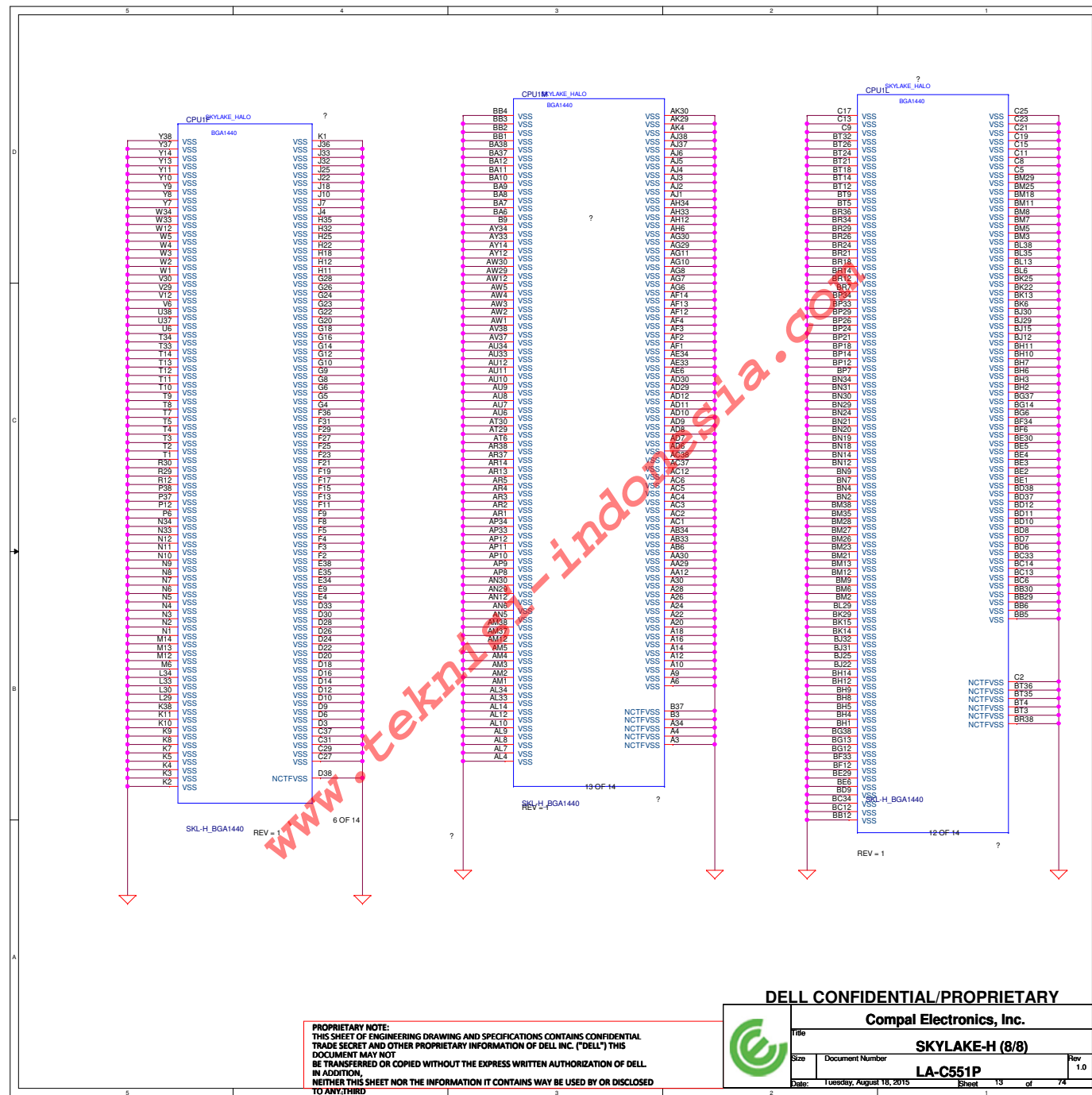
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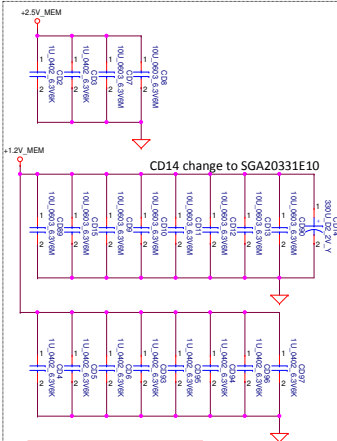




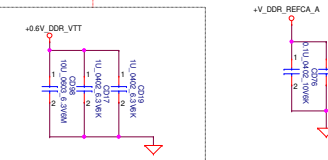


All VREF traces should have 10 mil trace width

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 <8.15> DDR\_A\_DQS[8..7] <>>  
 <8.15> DDR\_A\_DQ[0..63] <>>  
 <8.15> DDR\_A\_MA[0..13] <>>

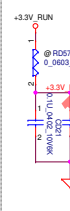
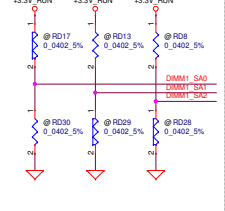


Layout Note:  
Place near JDIMM1.258

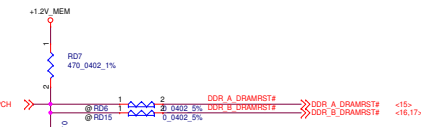
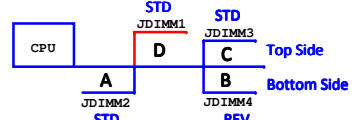


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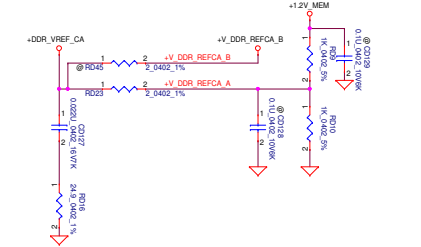
	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
DIMM1	1	0	0
DIMM3	1	1	0



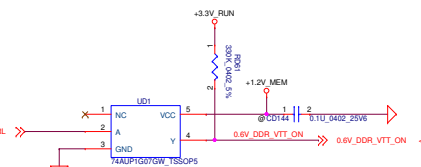
<7.15,16,17,23,41> DDR\_WD\_PAN\_SMBCLK <>>



<3> DDR\_A\_DRAMRST#\_PCH <>> <7.15,16,17,19,46>



<7> DDR\_PG\_CTRL <>> <7.15,16,17,23,41>



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DDRIII-SODIMM SLOT1

LA-C551P

Document Number

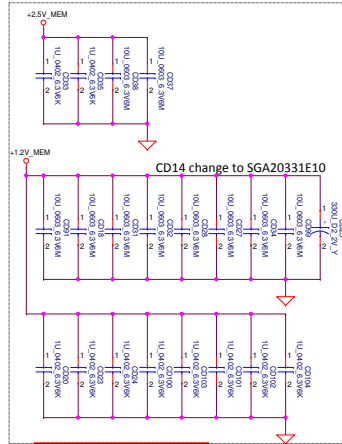
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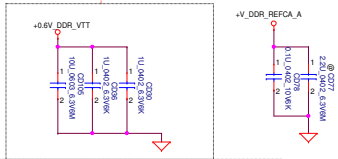
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# JDIMM2 STD Type H=4

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<B.14> DDR\_A\_DQS#8..7  
<B.14> DDR\_A\_DQ#0..63  
<B.14> DDR\_A\_MA#0..13

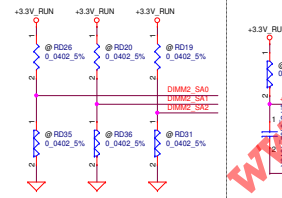


Layout Note:  
Place near JDIMM2.258



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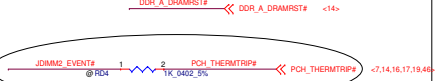
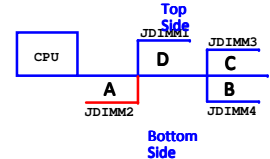
	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
DIMM1	1	0	0
DIMM3	1	1	0



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<7.14.16.17.23.41> DDR\_XDP\_WAL\_SMBCLK <7.14.16.17.23.41>  
<7.14.16.17.23.41> DDR\_XDP\_WAL\_SMBDAT <7.14.16.17.23.41>

L0TES\_ADDR106-P005A  
CONN@



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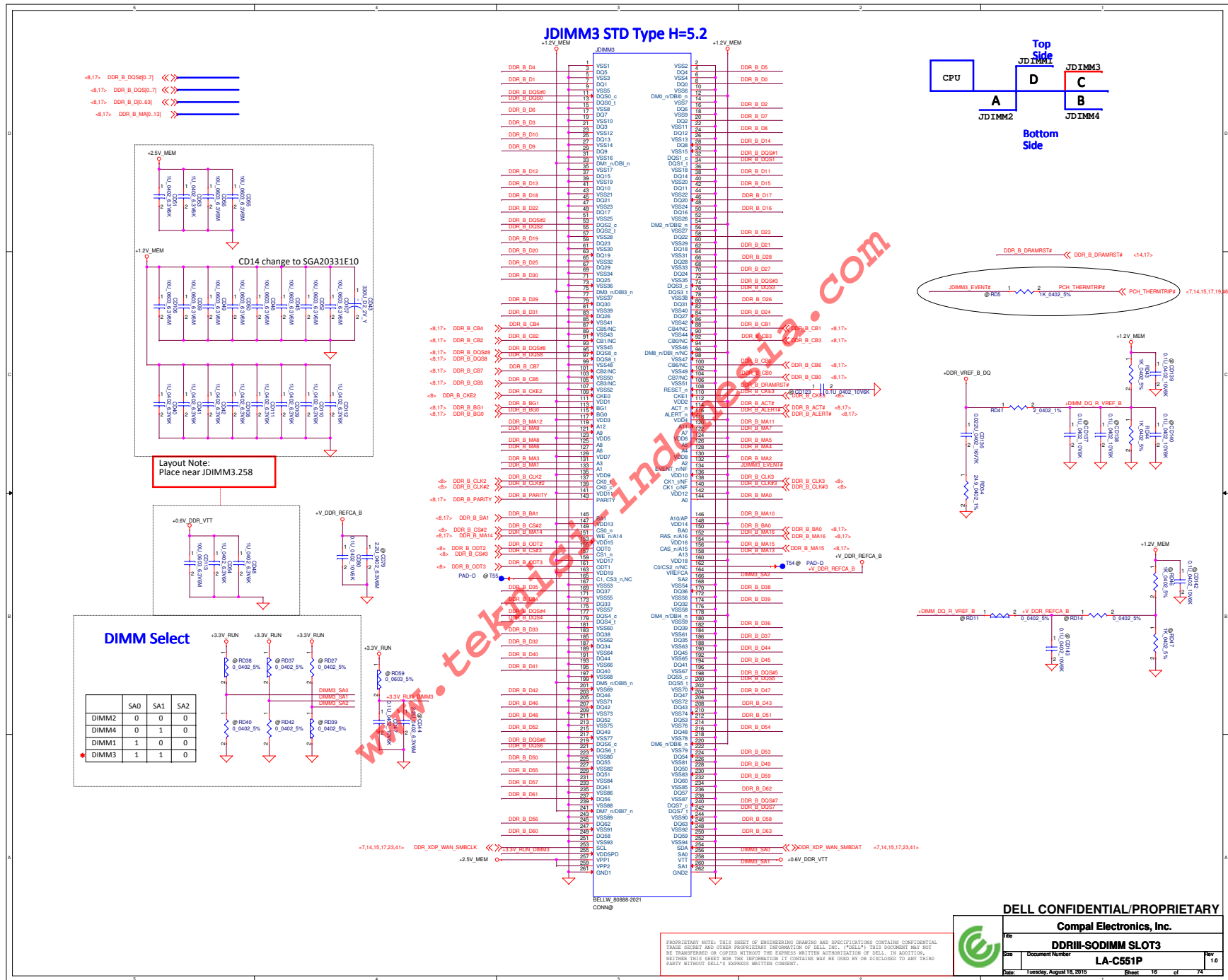
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DDRIII-SODIMM SL02

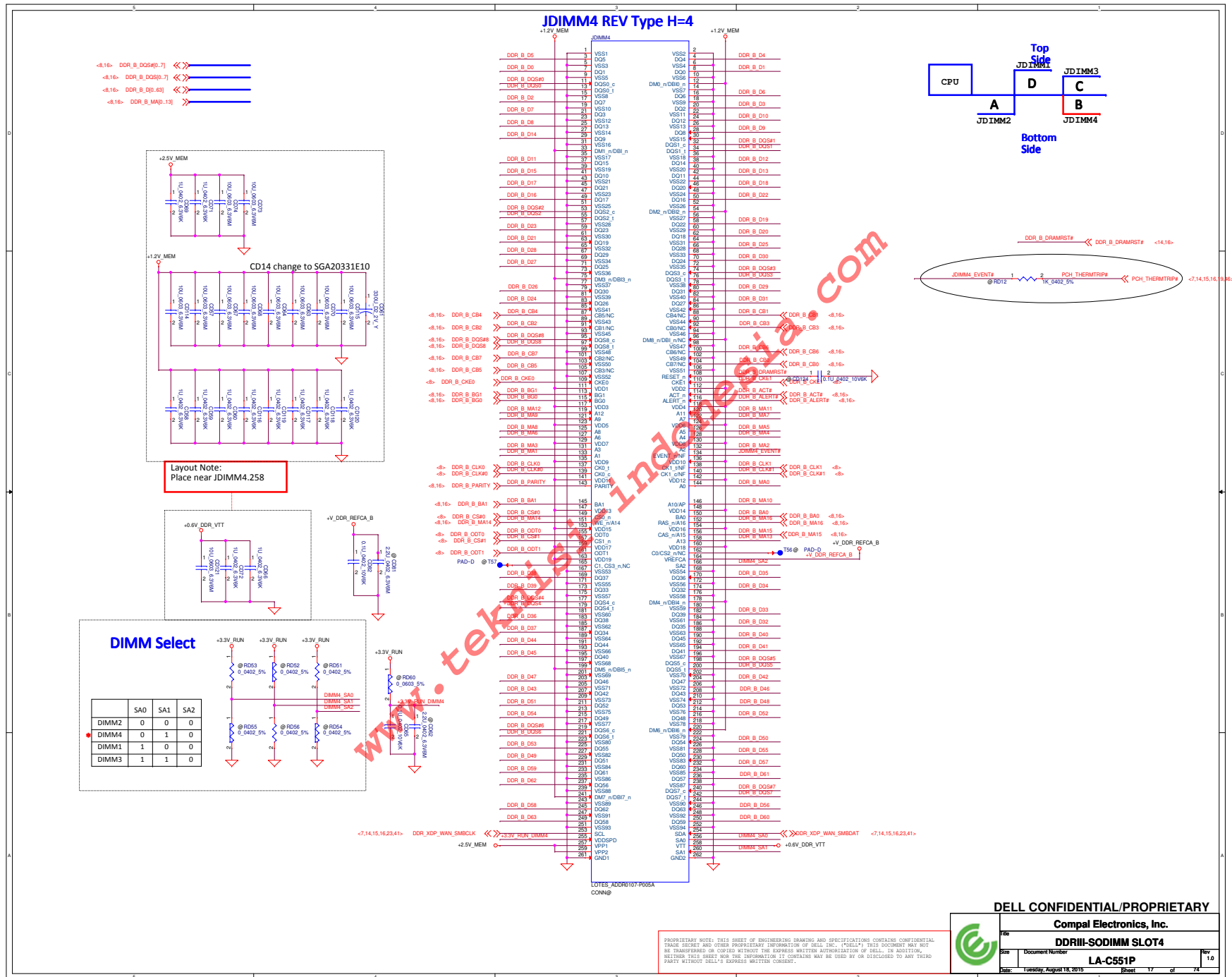
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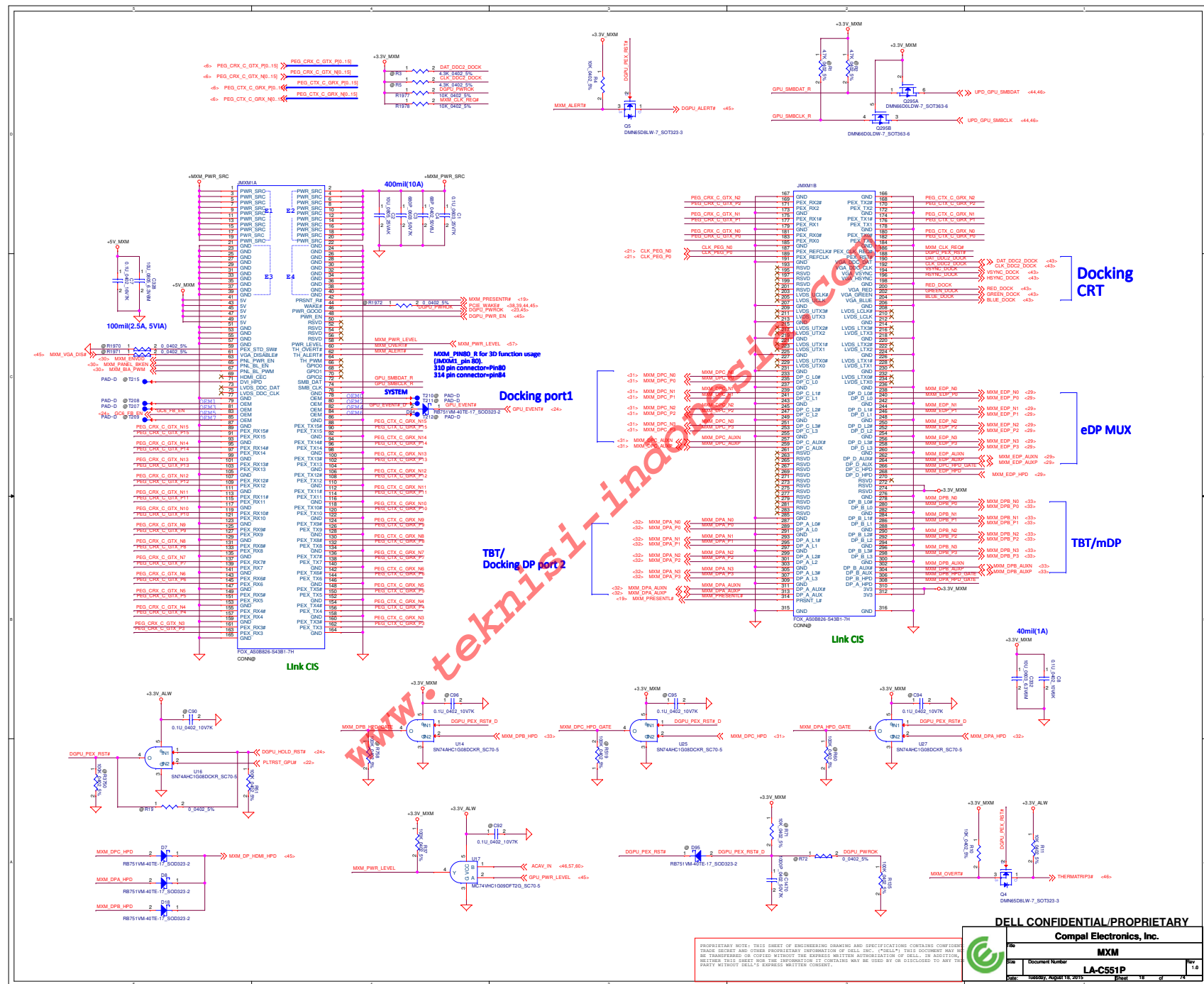
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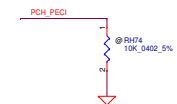
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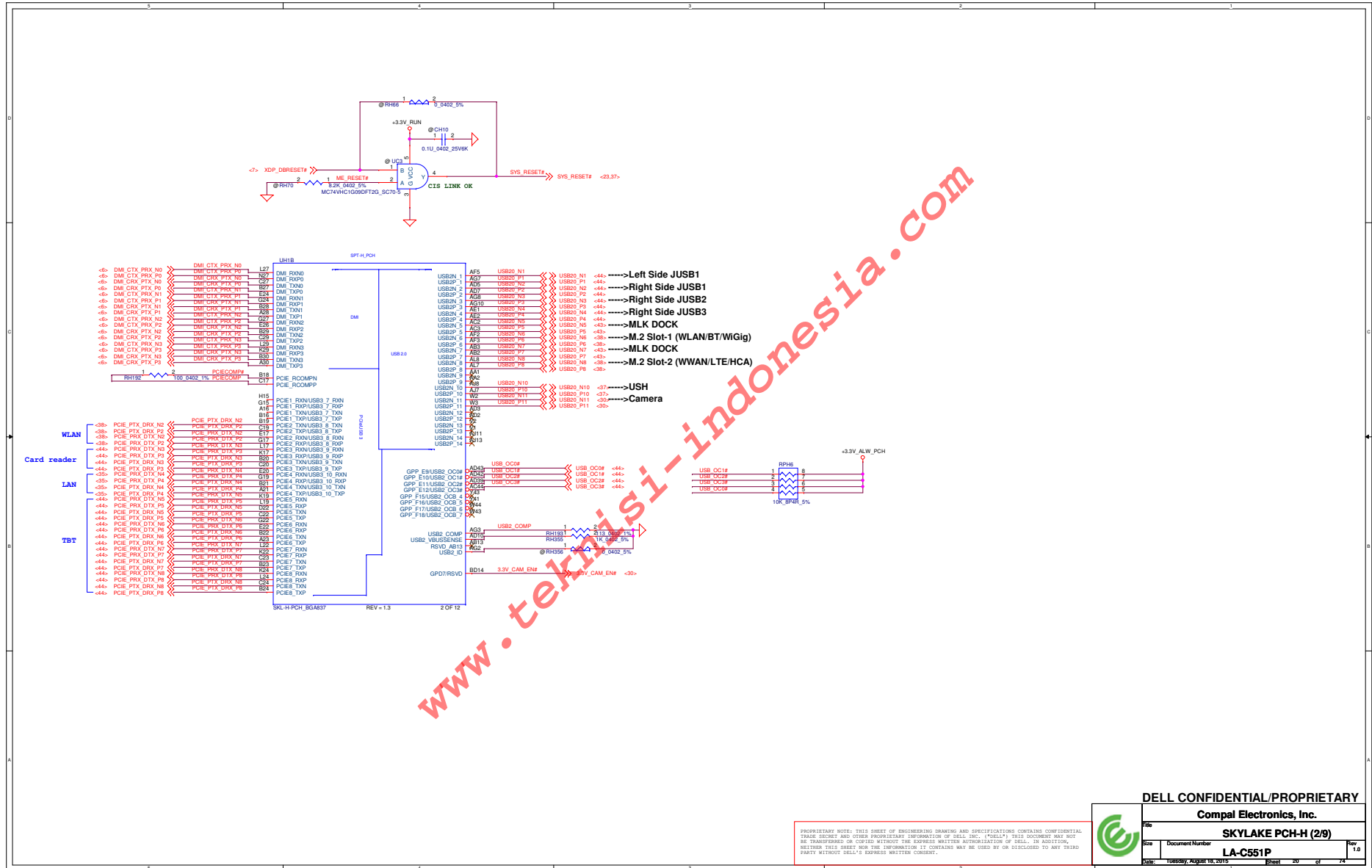




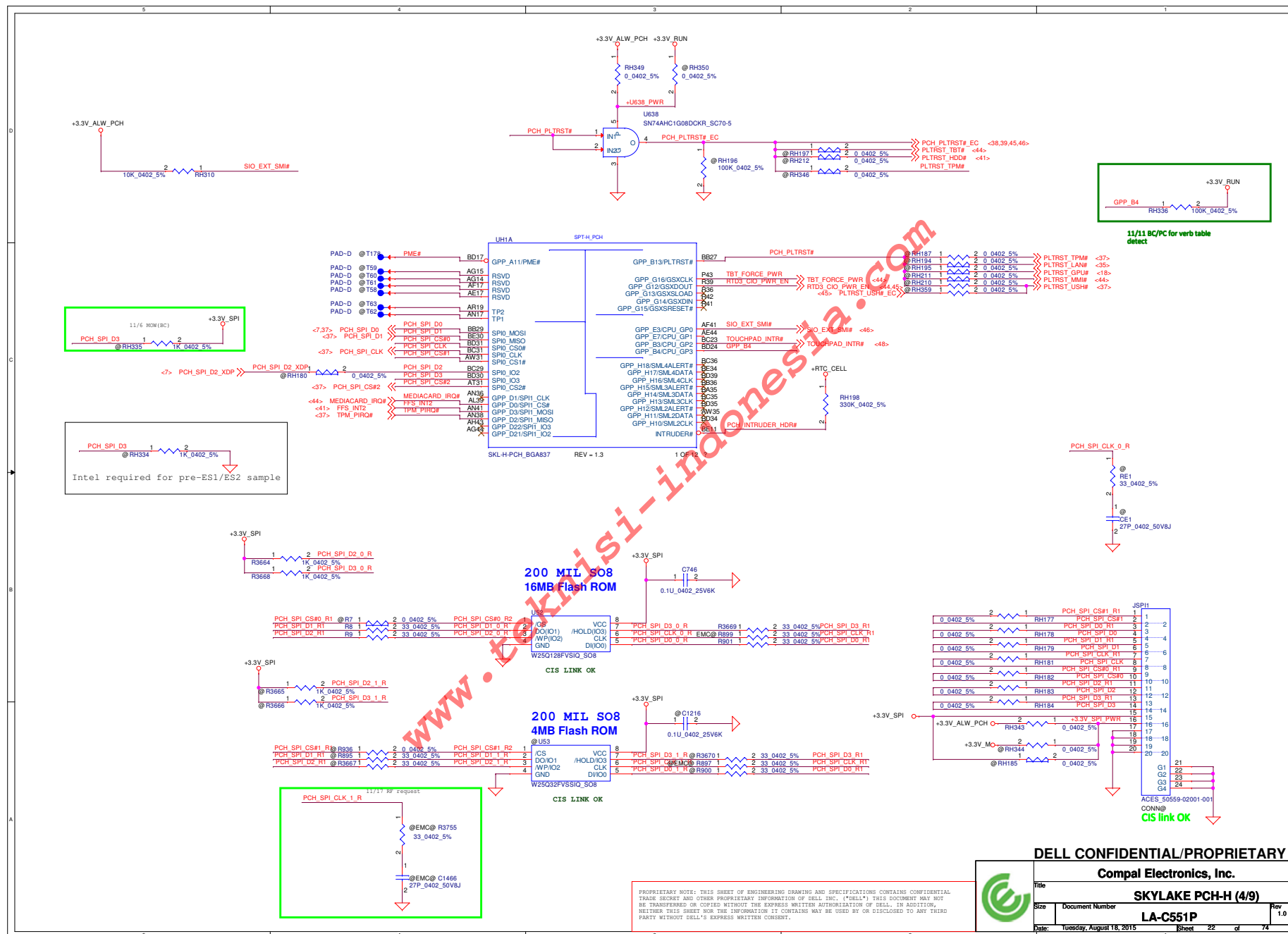






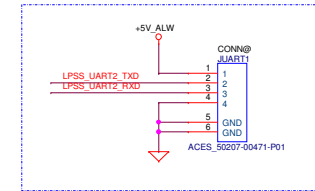
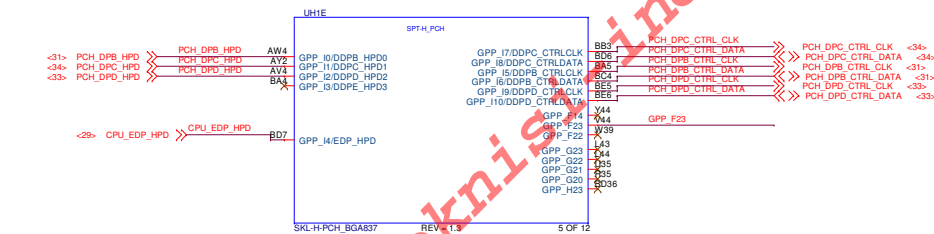
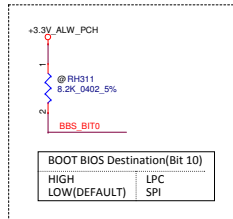
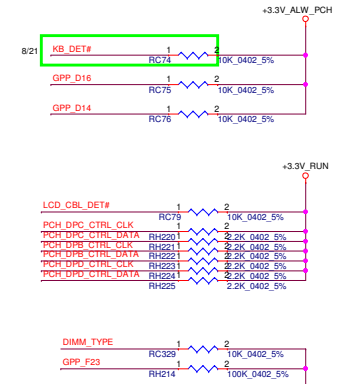
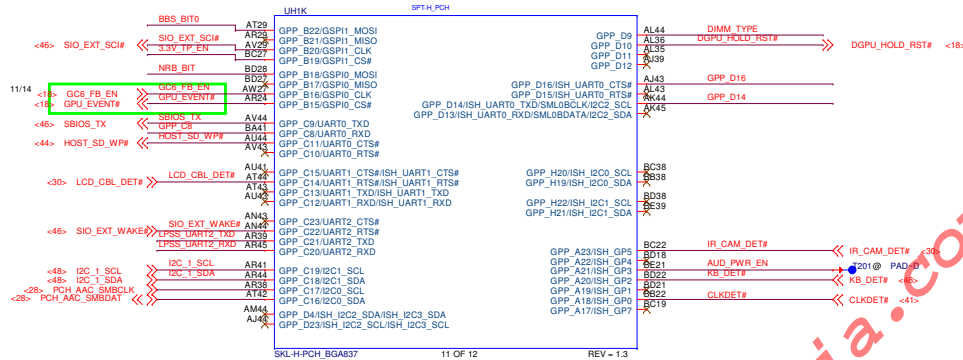
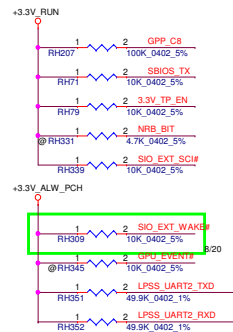












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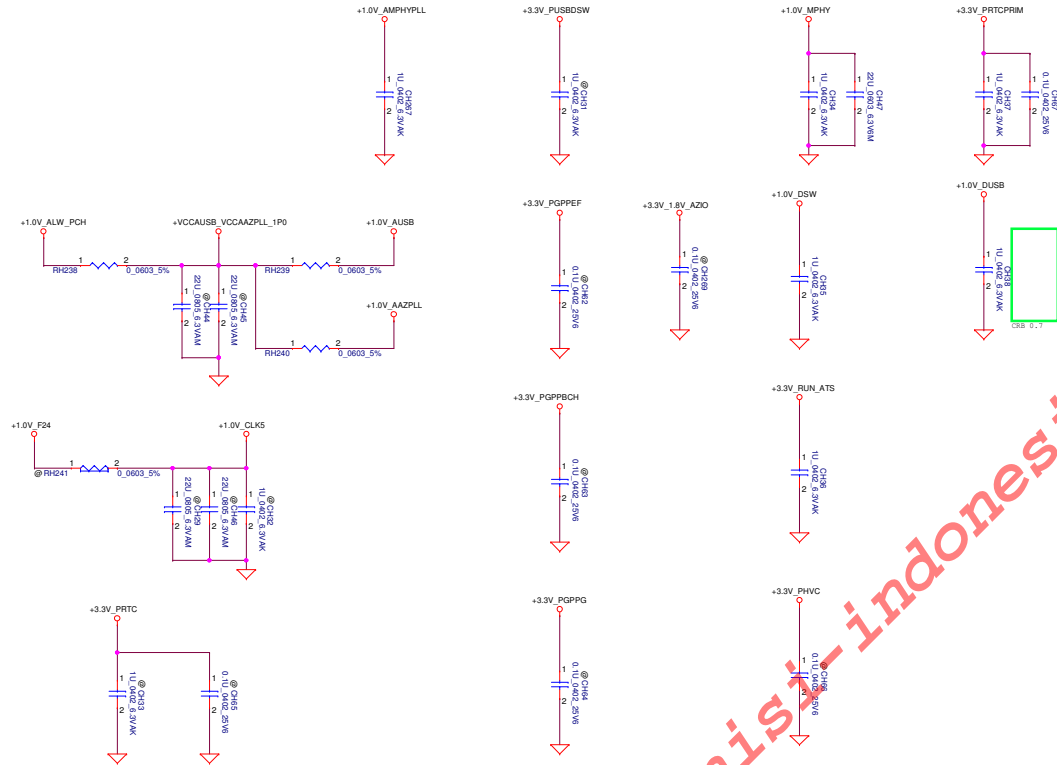
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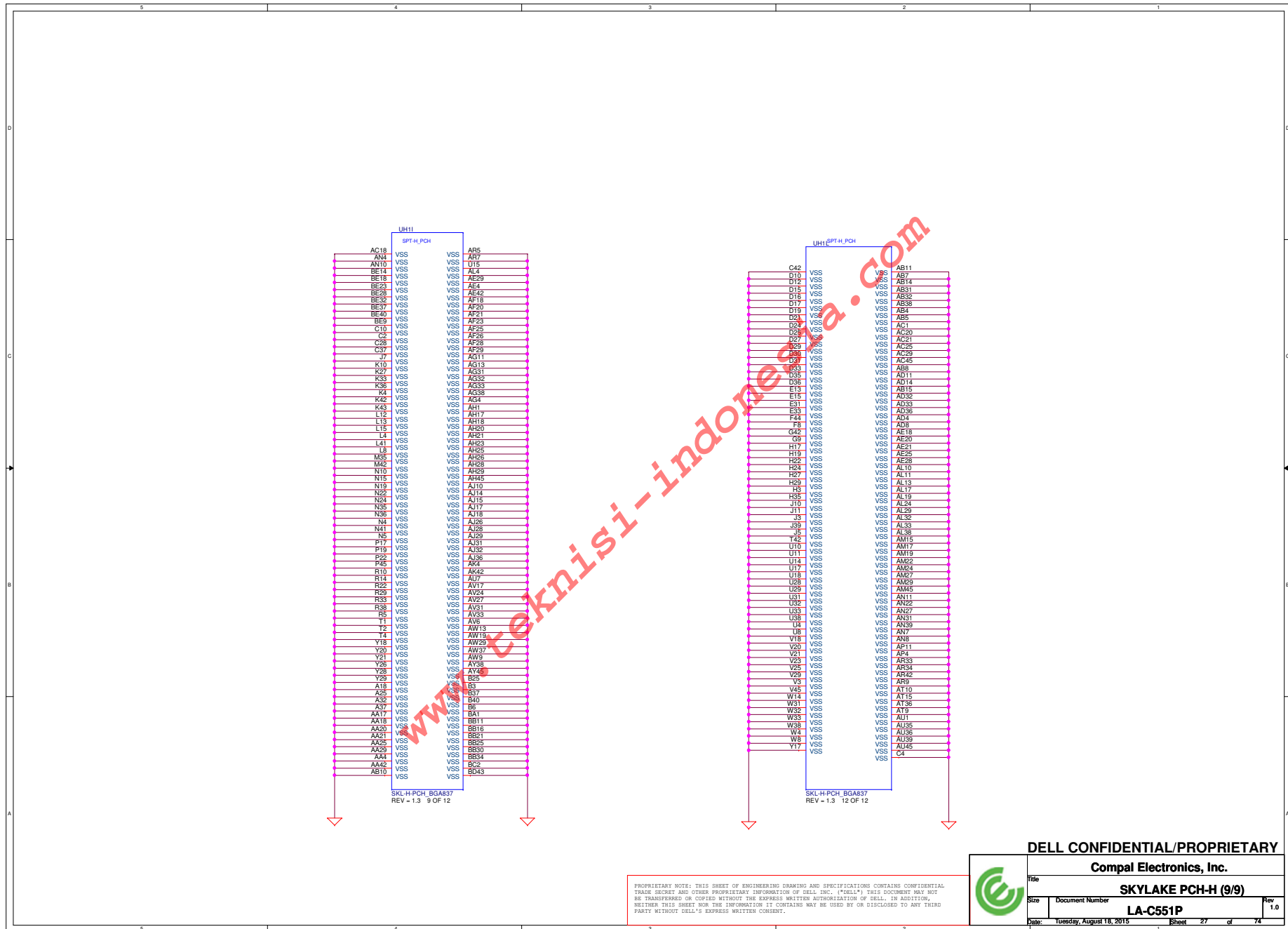
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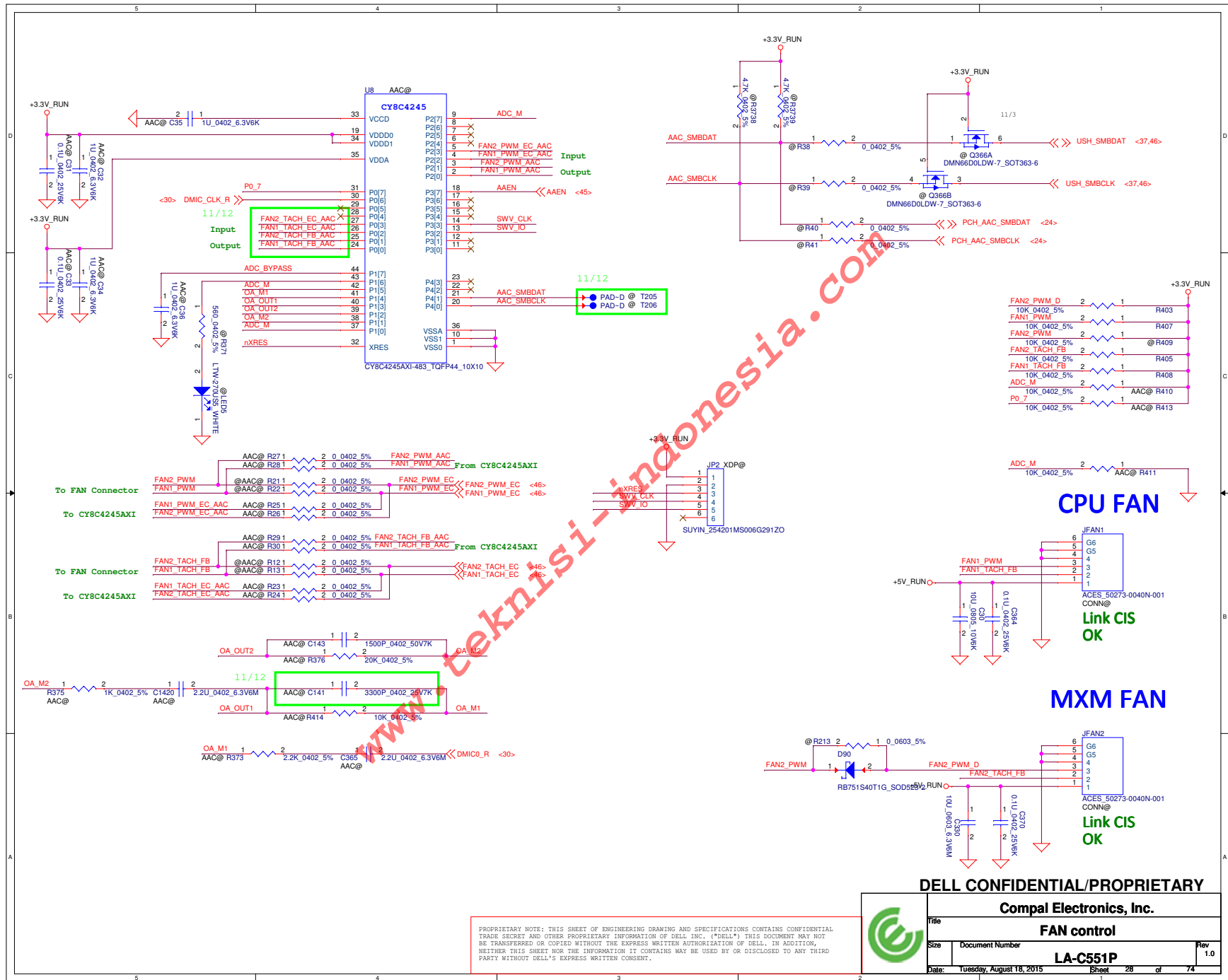
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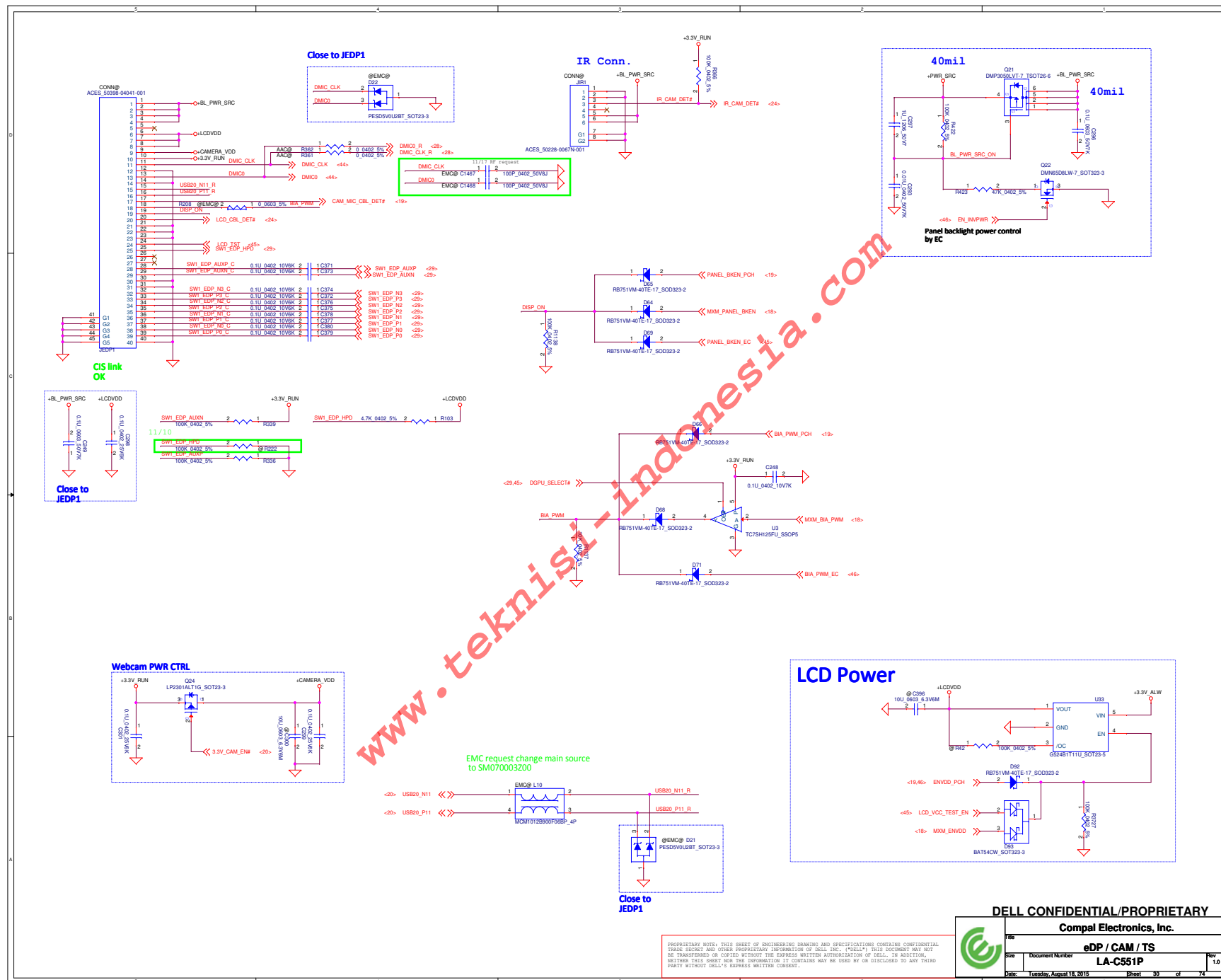
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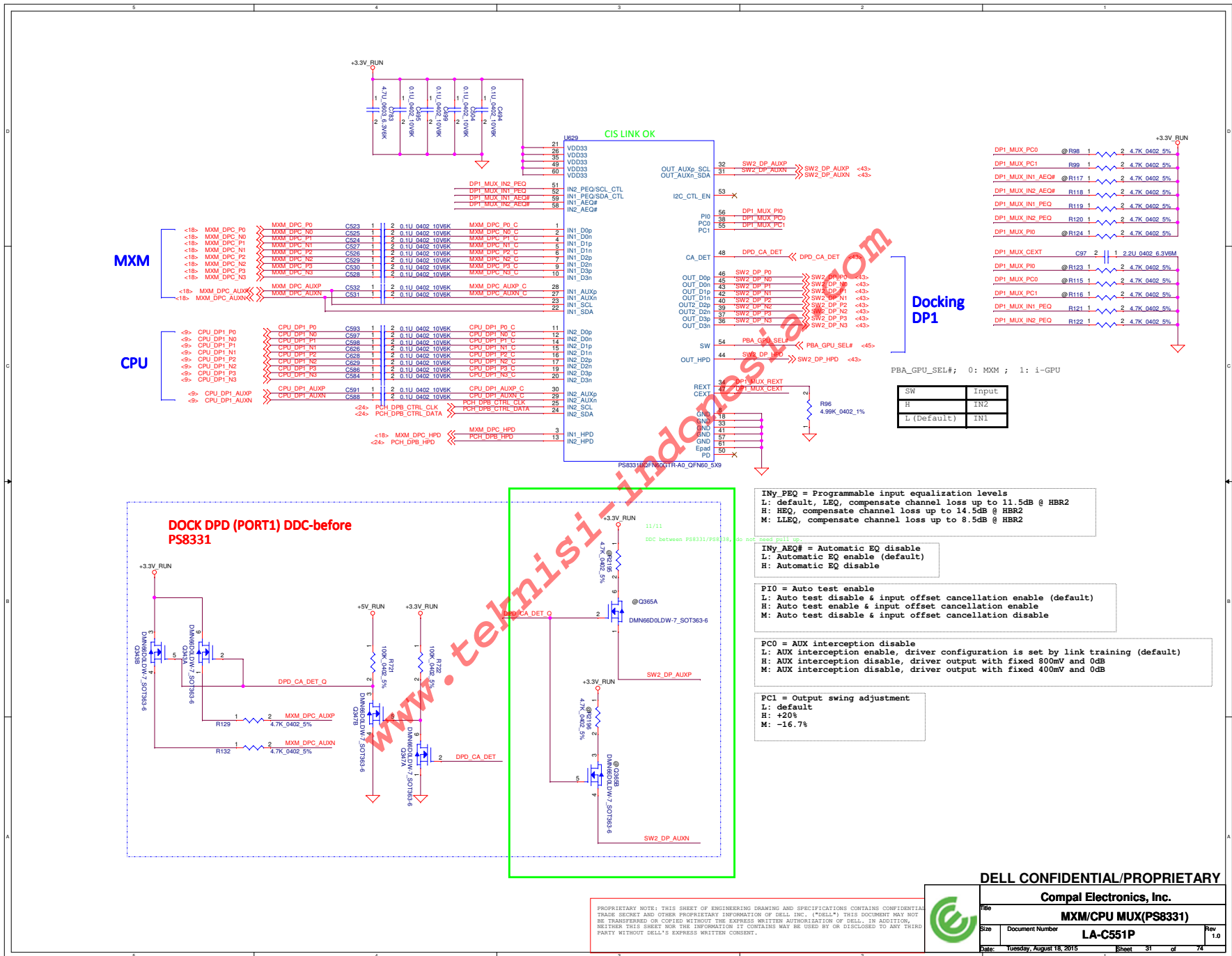
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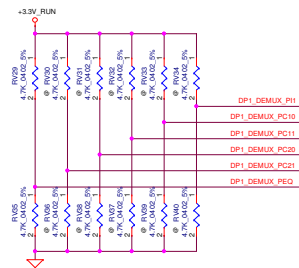
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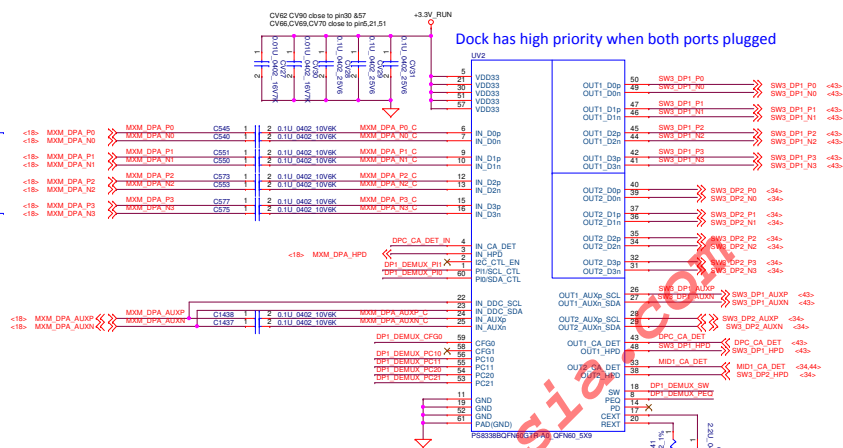








MXM



Dock has high priority when both ports plugged

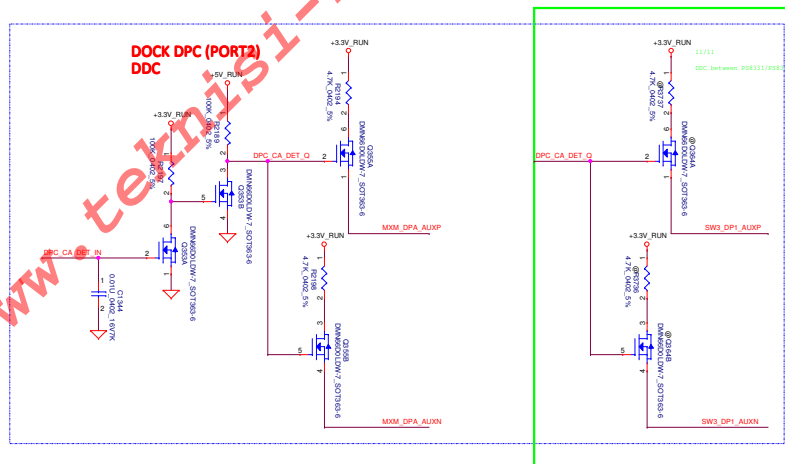
## Docking port2

MUX

Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O

For Control Switching Mode (CFG0 = L):  
SW = L: Port1 is selected (default)  
SW = H: Port2 is selected

For Automatic Switching Mode (CFG0 = H): (By OUT1\_HPD and OUT2\_HPD)  
SW = L: Port1 has higher priority when both ports are plugged (default)  
SW = H: Port2 has higher priority when both ports are plugged



DCC between P28331/P28336. Do not seed pull up

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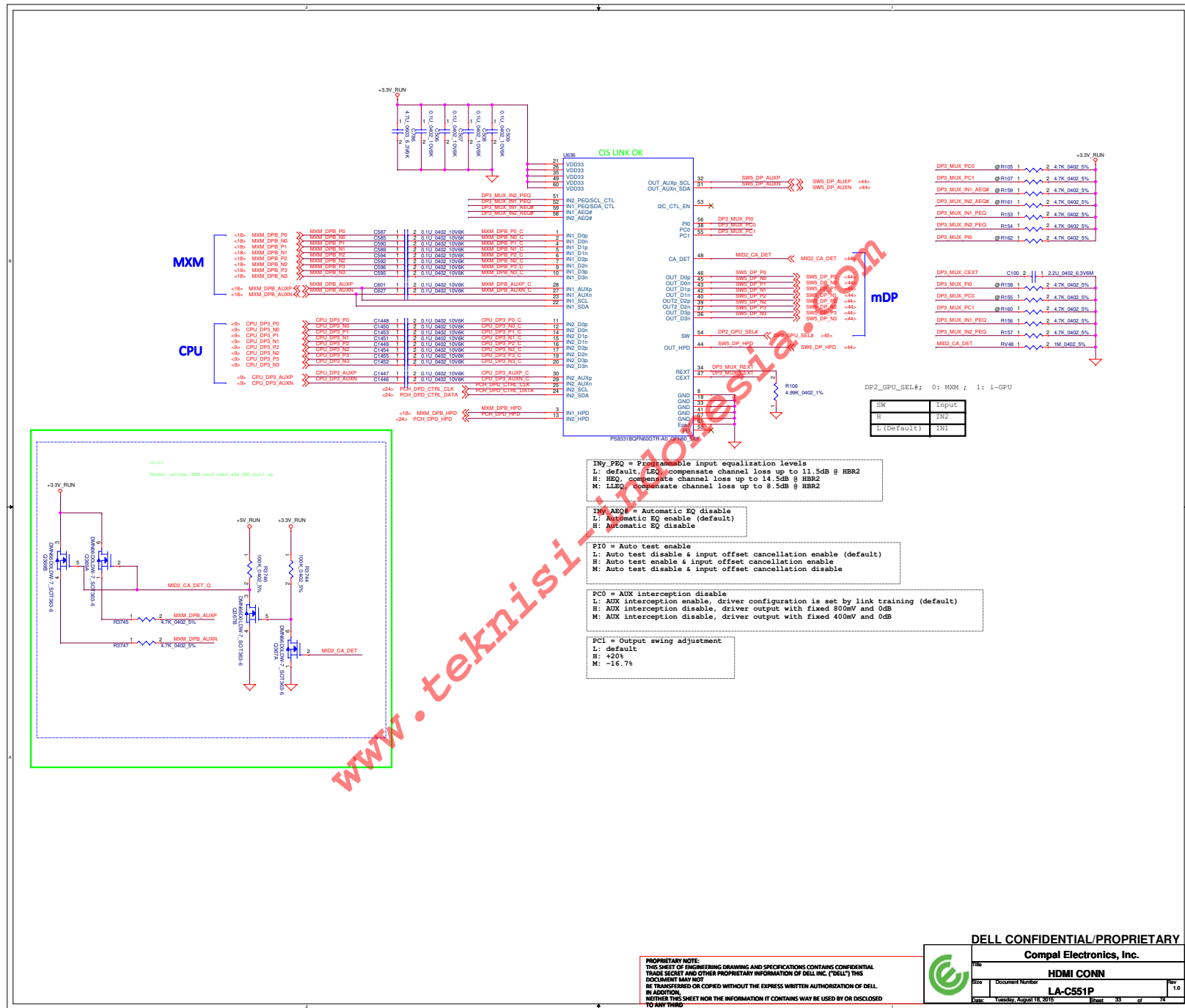
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**DP DeMUX (PS8338)**

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MUX

CPU

INy PEQ = Programmable input equalization levels  
L: default, LFEQ, compensate channel loss up to 11.5dB @ HBR2  
H: HEQ, compensate channel loss up to 14.5dB @ HBR2  
M: LFEQ, compensate channel loss up to 9.5dB @ HBR2

INy AEG# = Automatic EQ disable  
L: Automatic EQ enable (default)  
H: Automatic EQ disable

PI0 = Auto test enable  
L: Auto test disable & input offset cancellation enable (default)  
H: Auto test enable & input offset cancellation enable  
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable  
L: AUX interception enable, driver configuration is set by link training (default)  
H: AUX interception disable, driver output with fixed 800mV and 0dB  
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment  
L: default  
H: +20%  
M: -15.7%

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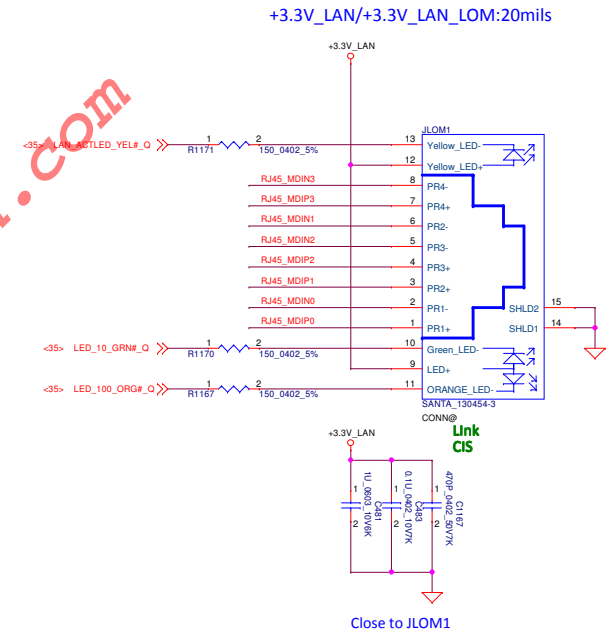
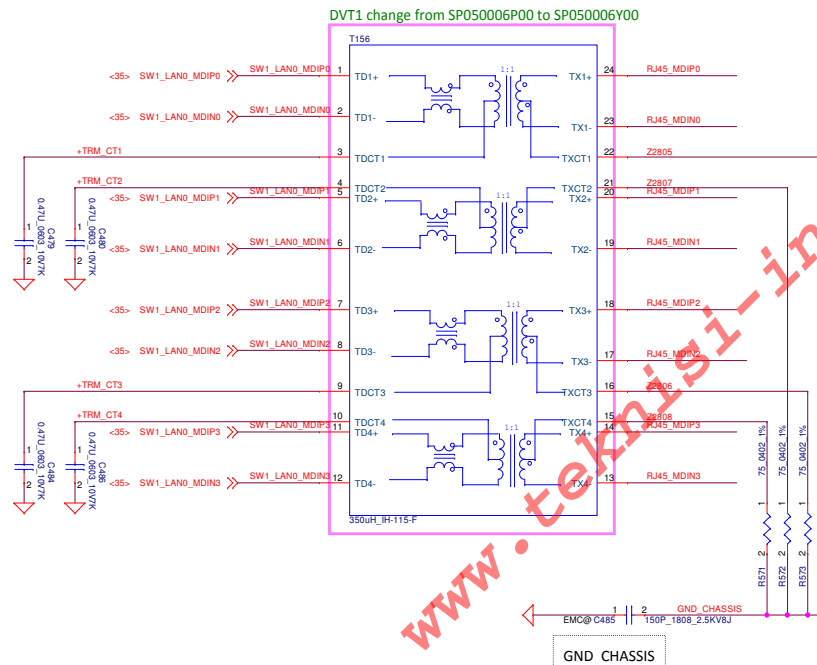


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Rev	VGA CONN		
Doc#	Document Number	LA-C551P	
Rev	1.0		

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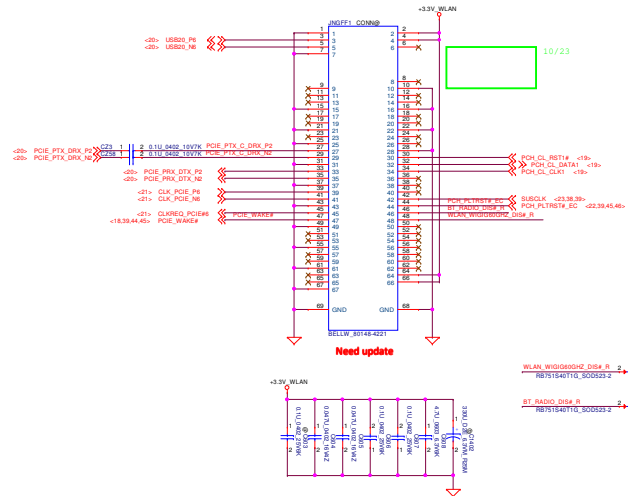


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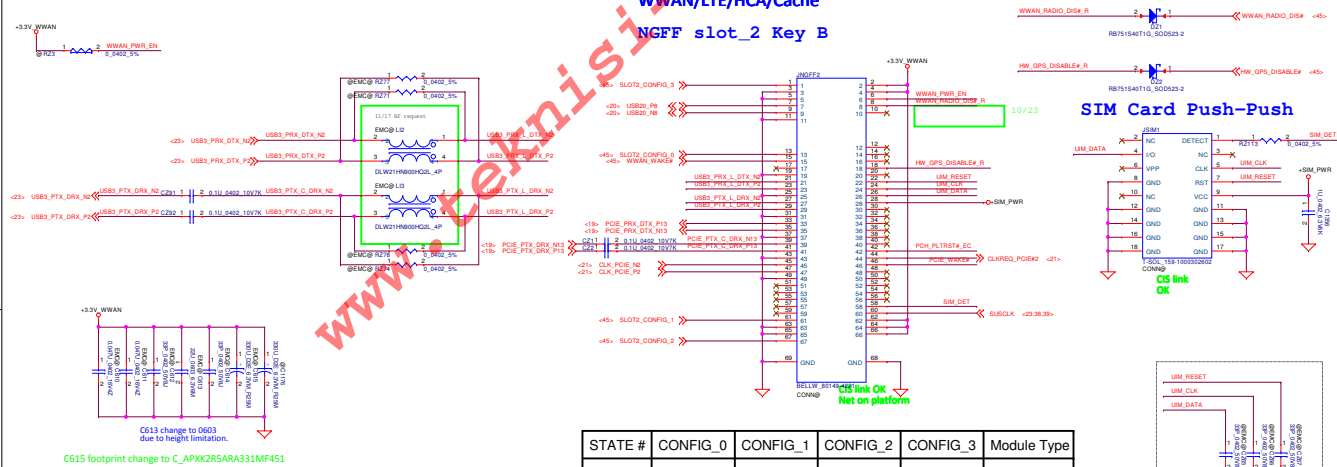
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Compal Electronics, Inc.			
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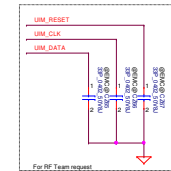
WLAN/BT/WiGig  
NGFF slot\_1 Key A



WWAN/LTE/HCA/Cache  
NGFF slot\_2 Key B



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	0	0	0	0	SSD-SATA
8	1	0	0	0	WWAN
14	1	0	1	1	HCA-PCIE
15	1	1	1	1	Cache



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**M.2 Card-1/2**

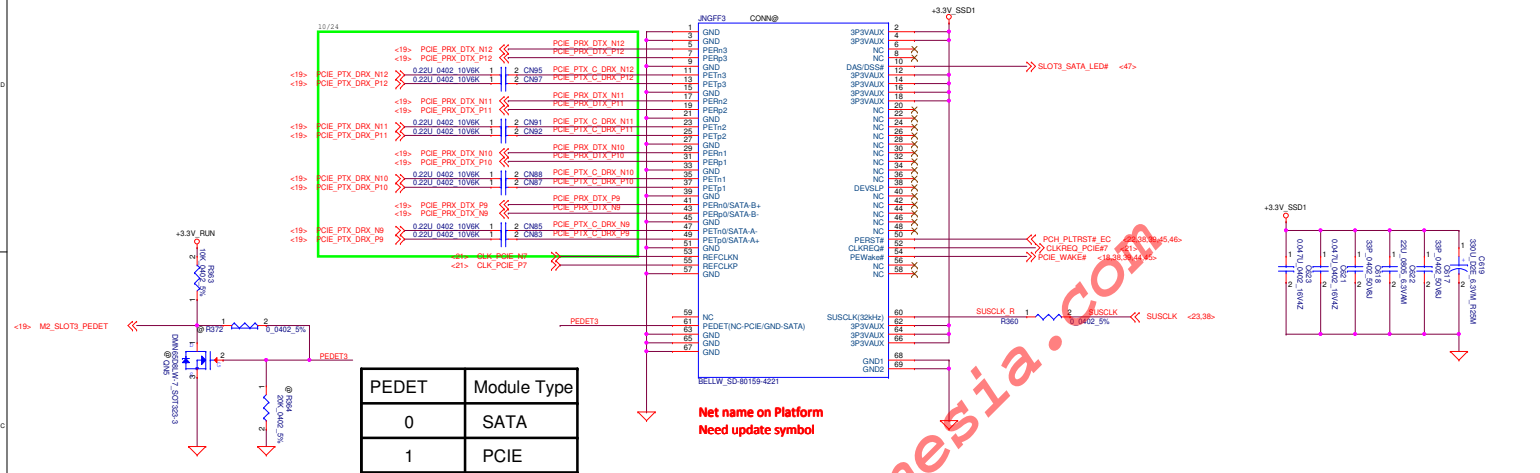
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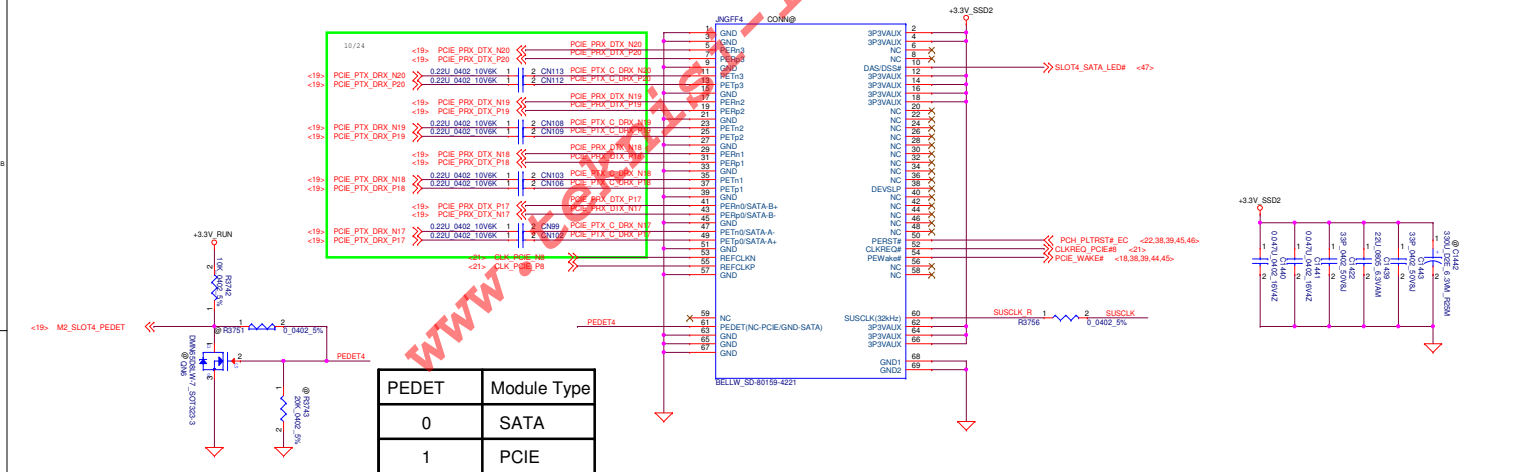
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# SSD NGFF slot\_3 Key M



# SSD NGFF slot\_4 Key M



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M.2 Card-2/2

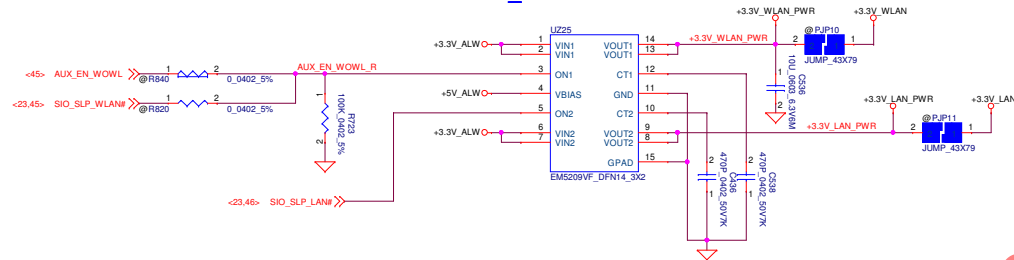
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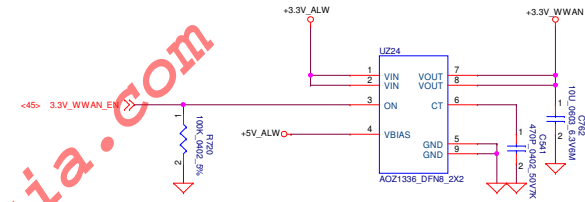
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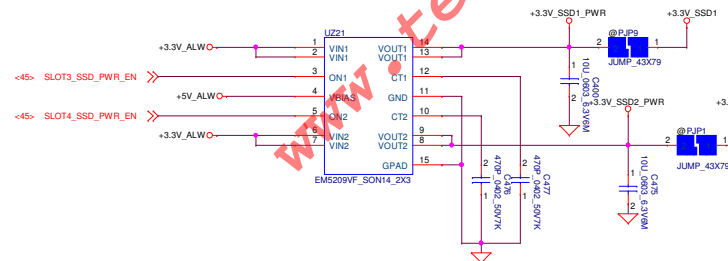
### Power Control for M.2 slot 1. & +3.3V\_RUN Source



### Power Control for M.2 slot 2.



### Power Control for M.2 slot 3. Source Power Control for M.2 slot 4. Source



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M.2 Card PWR

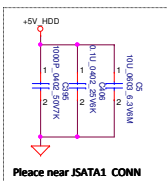
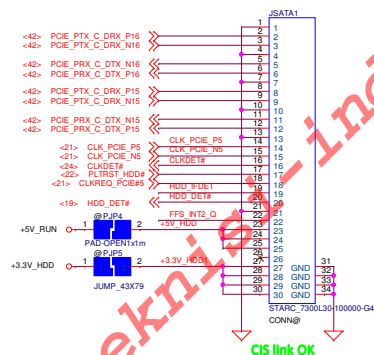
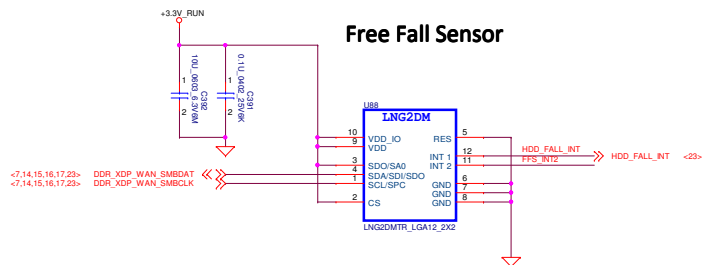
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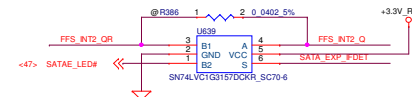
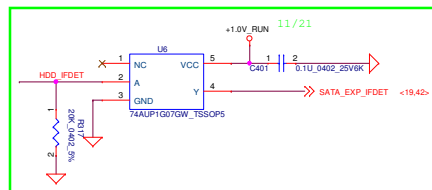
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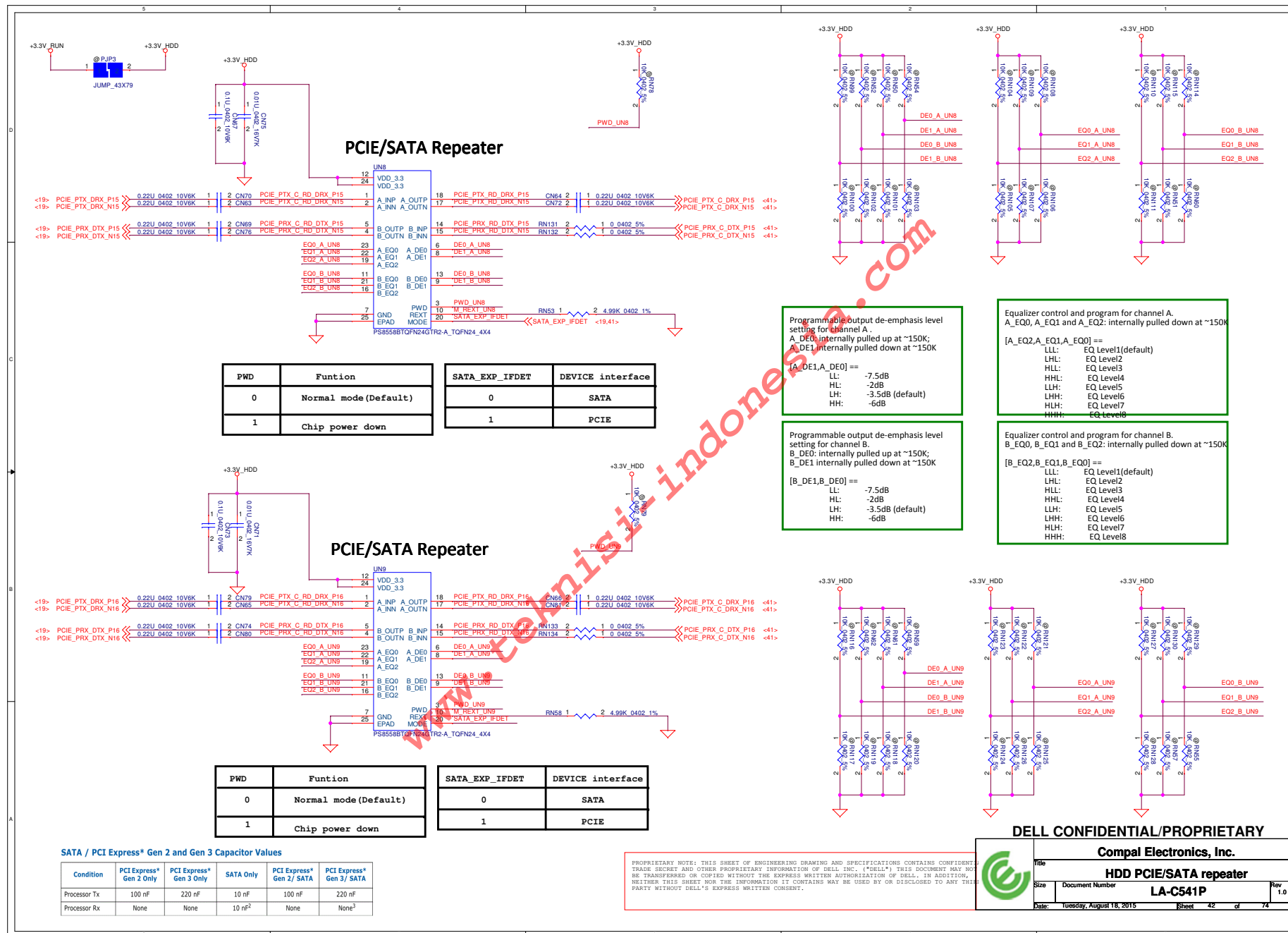


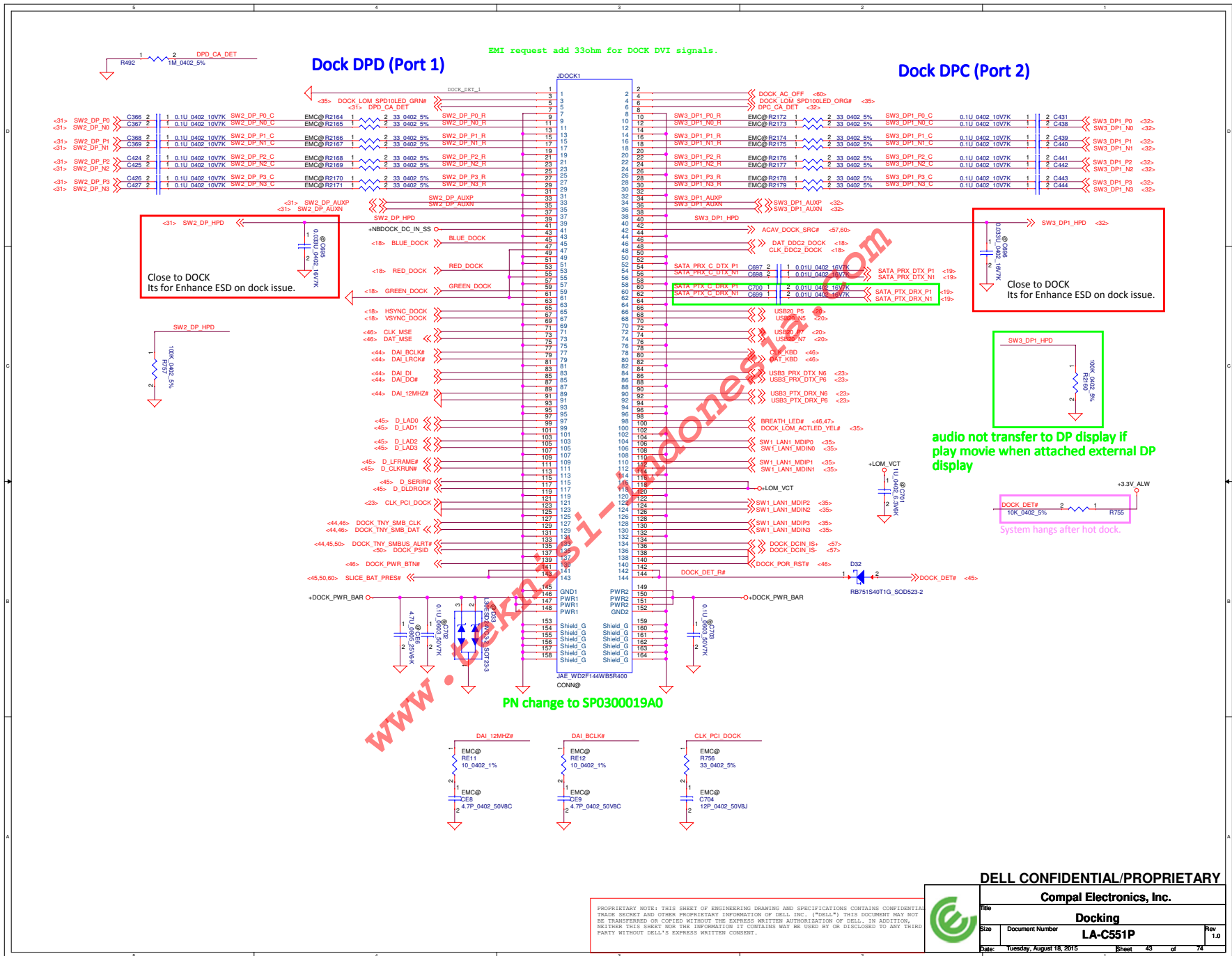


SATA_EXP_IFDET	DEVICE interface
0	SATA
1	PCIE

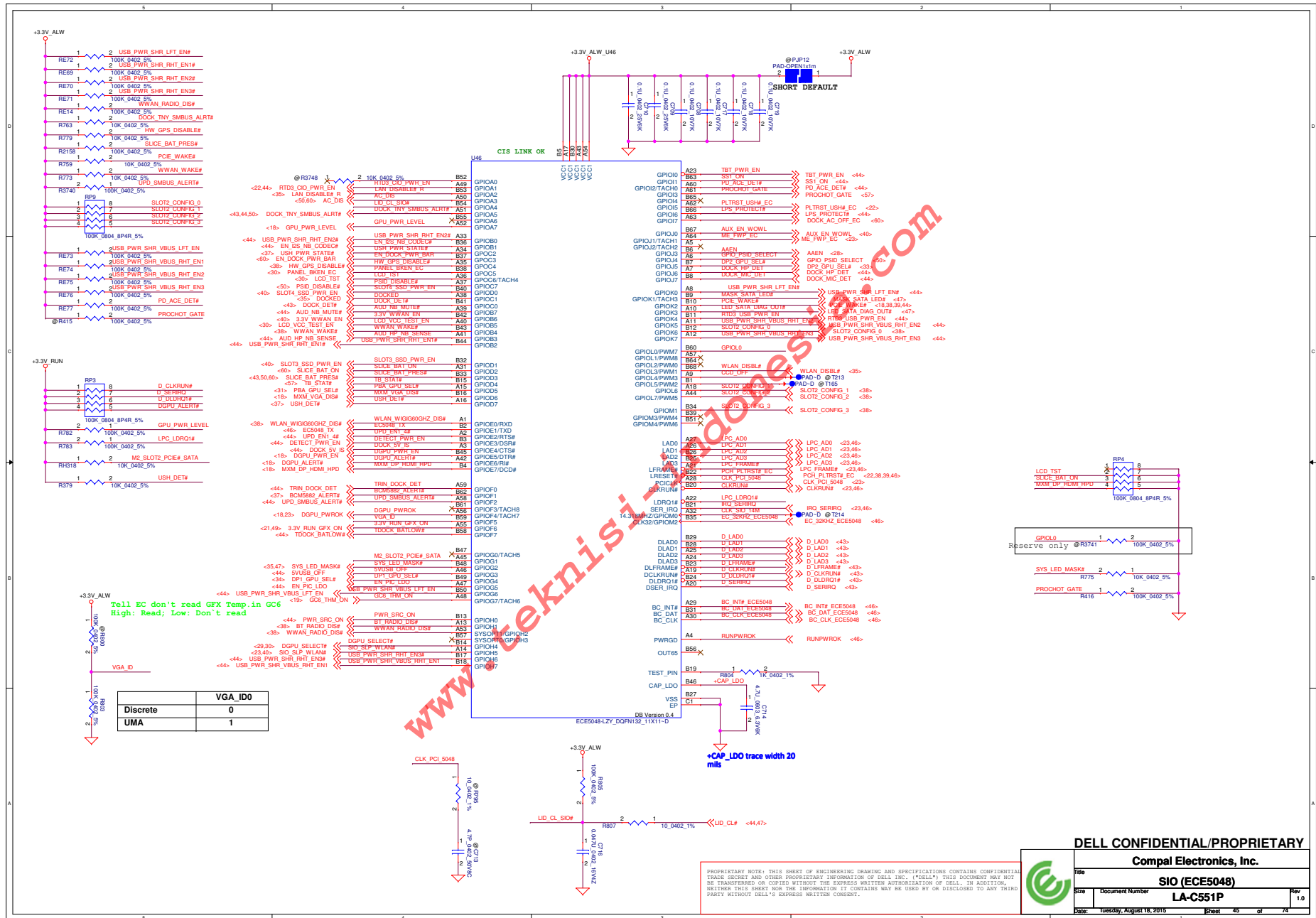
SATA_EXP_IFDET	channel on
0	A-->B1
1	A-->B2

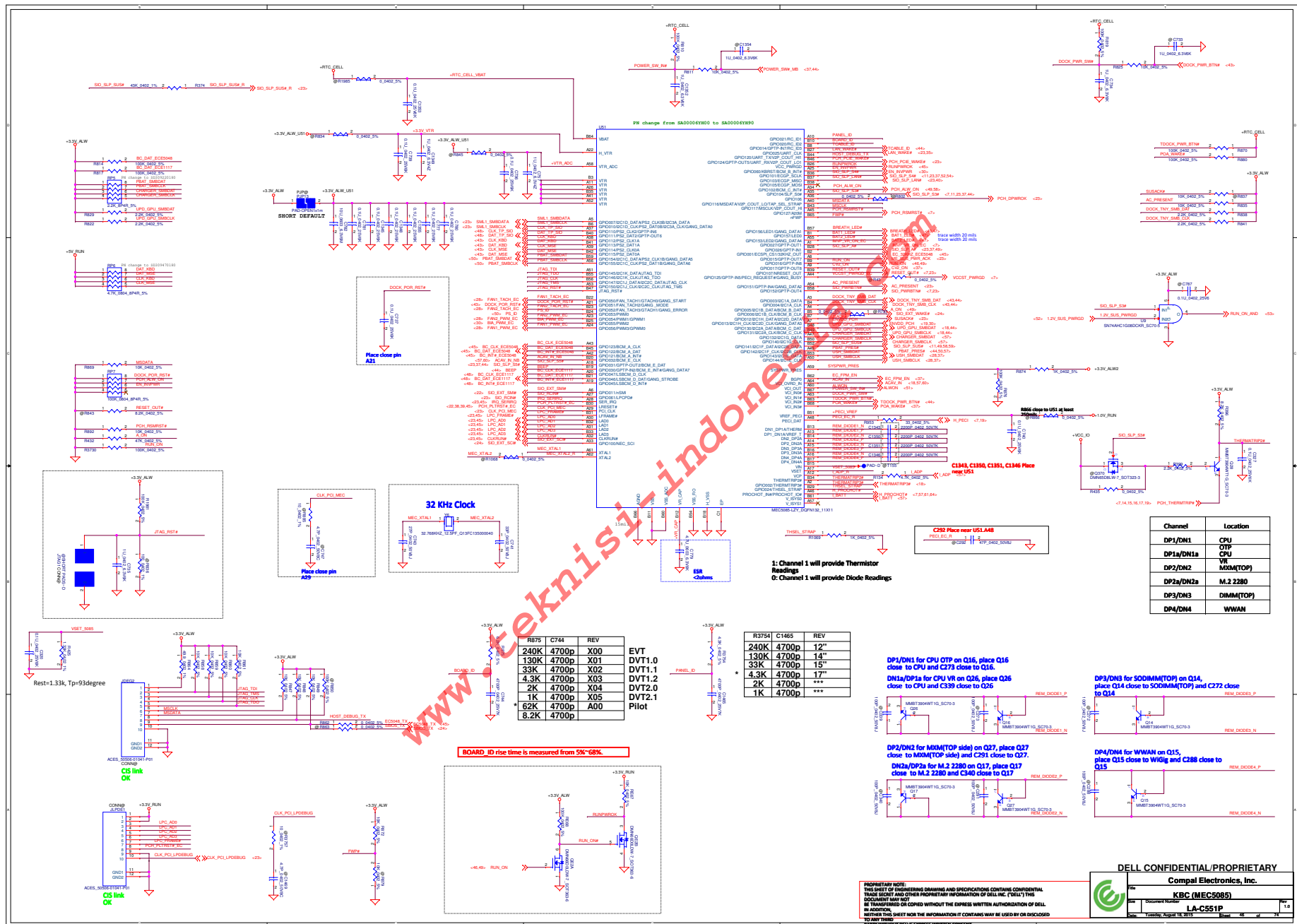


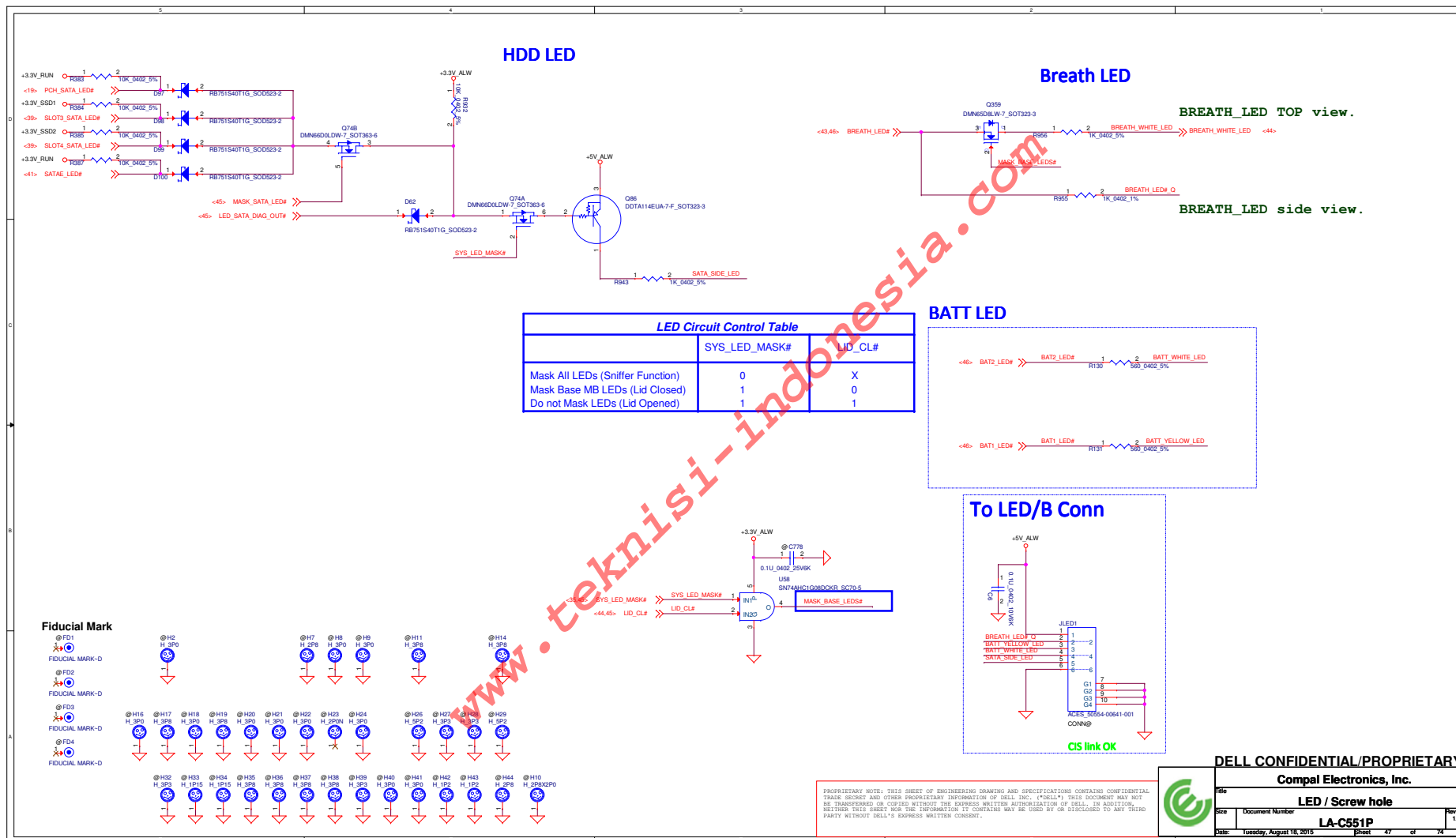




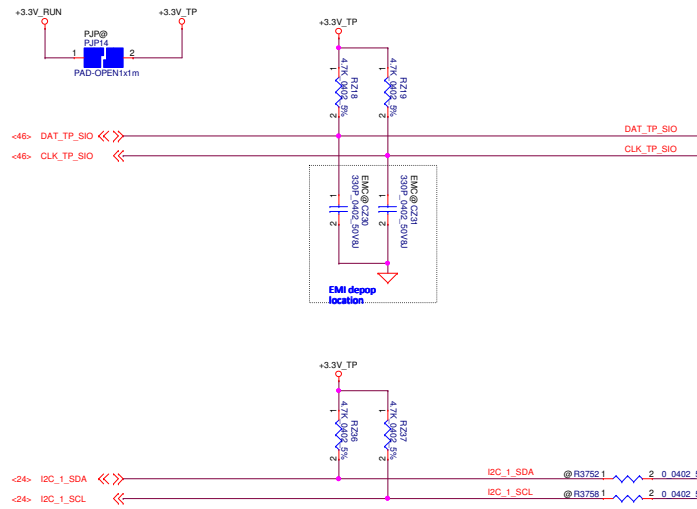




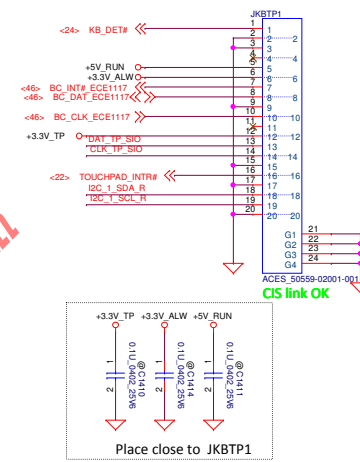




## Touch Pad



## Keyboard



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Compal Electronics, Inc.

KB / TP / RSMRST#

LA-C551P

Size

Document Number

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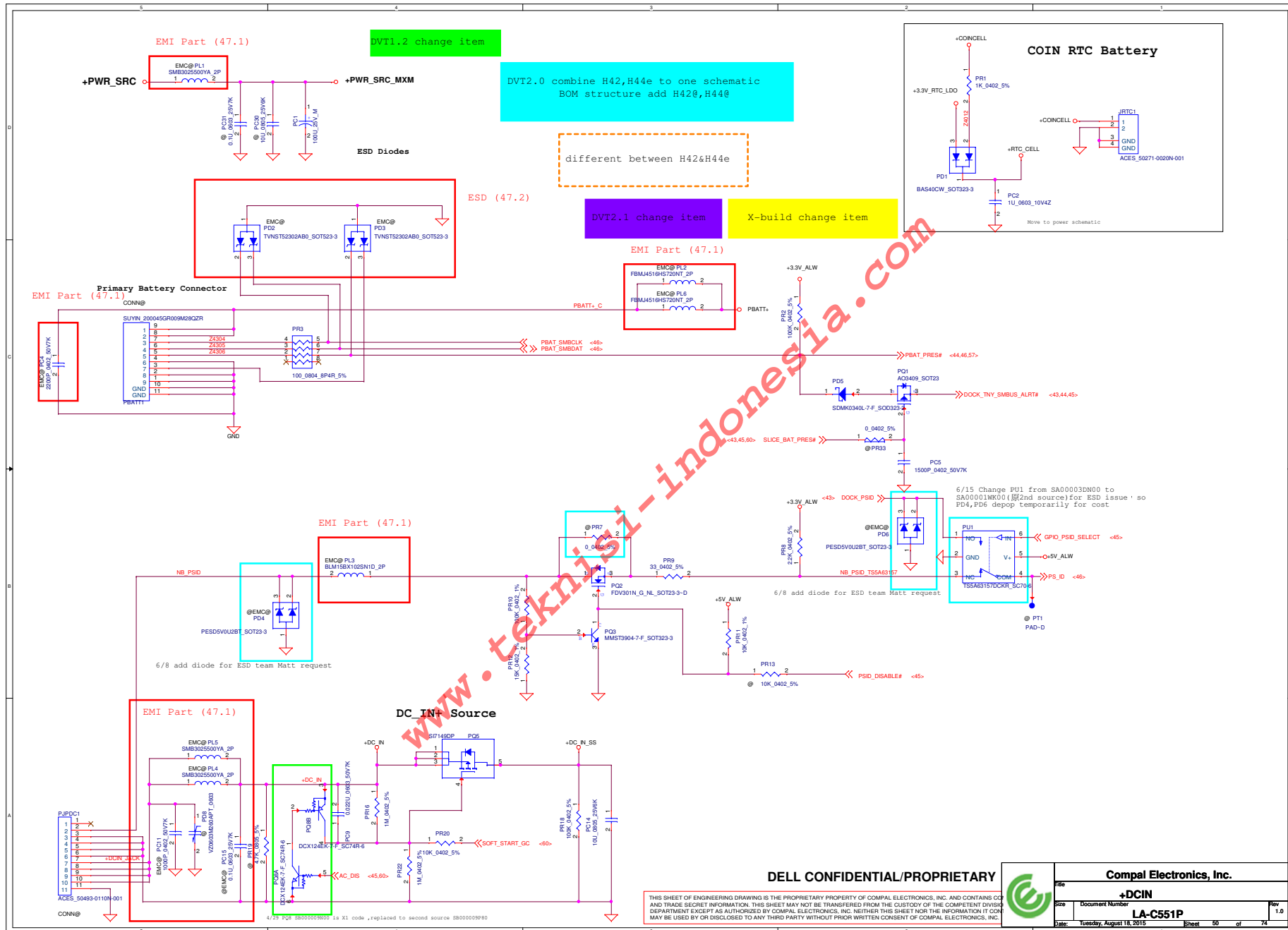
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+PWR\_SRC

+3.3V\_ALW

+3.3V\_ALW

+VCC\_IO  
TDC 3.85A  
Peak Current 5.5 A  
OCP Current 8 A  
TYP  
MAX  
Choke DCR 13.0mohm ,  
14.0mohm

+VCC\_IOP

+VCC\_IO

PJP300  
PAD-OPEN 43x118

+VCC\_IOP

proximal  
PR311 0 ohm PR314 10 ohm PR316 10 ohm  
remote  
PR311 10 ohm PR314 0 ohm PR316 0 ohm

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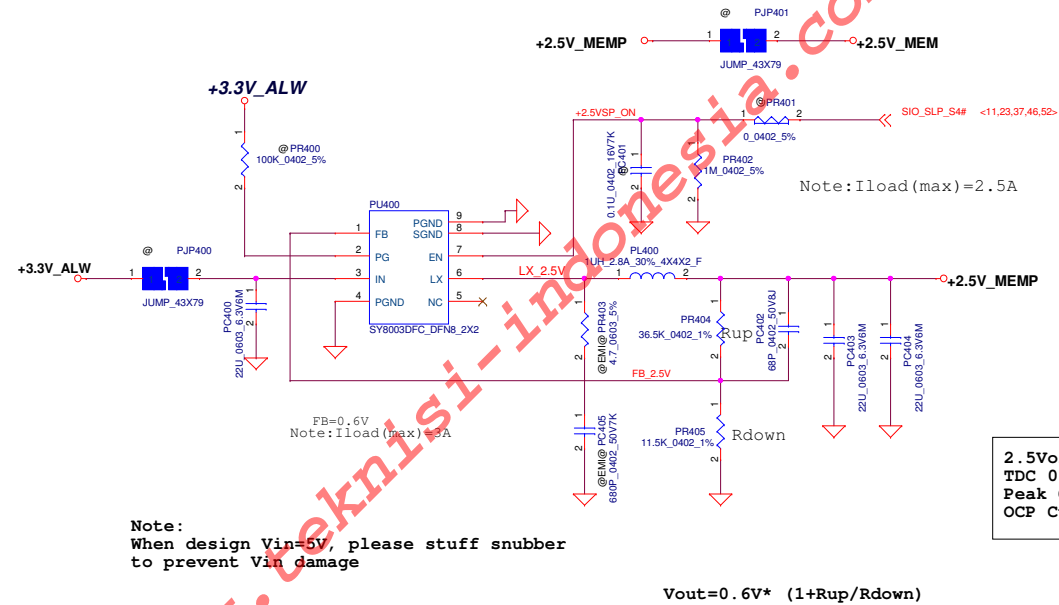
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+VCC\_IO 0.95V

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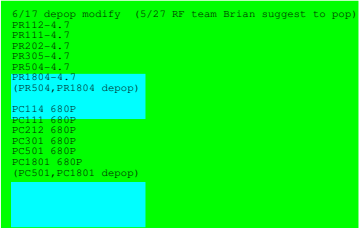
**Note:**  
 When design Vin=5V, please stuff snubber  
 to prevent Vin damage

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Only H44e



+VCCEDRAM(+1.00V)  
TDC 2.31 A  
Peak Current 3.3 A  
OCP Current 8 A  
MAX  
Choke DCR 48.0mohm

proximal	PR505 0ohm	PR506 100ohm	PR508 100ohm
remote	PR505 100ohm	PR506 0ohm	PR508 0ohm

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+VCCEDRAM, 1V

**LA-C551P**

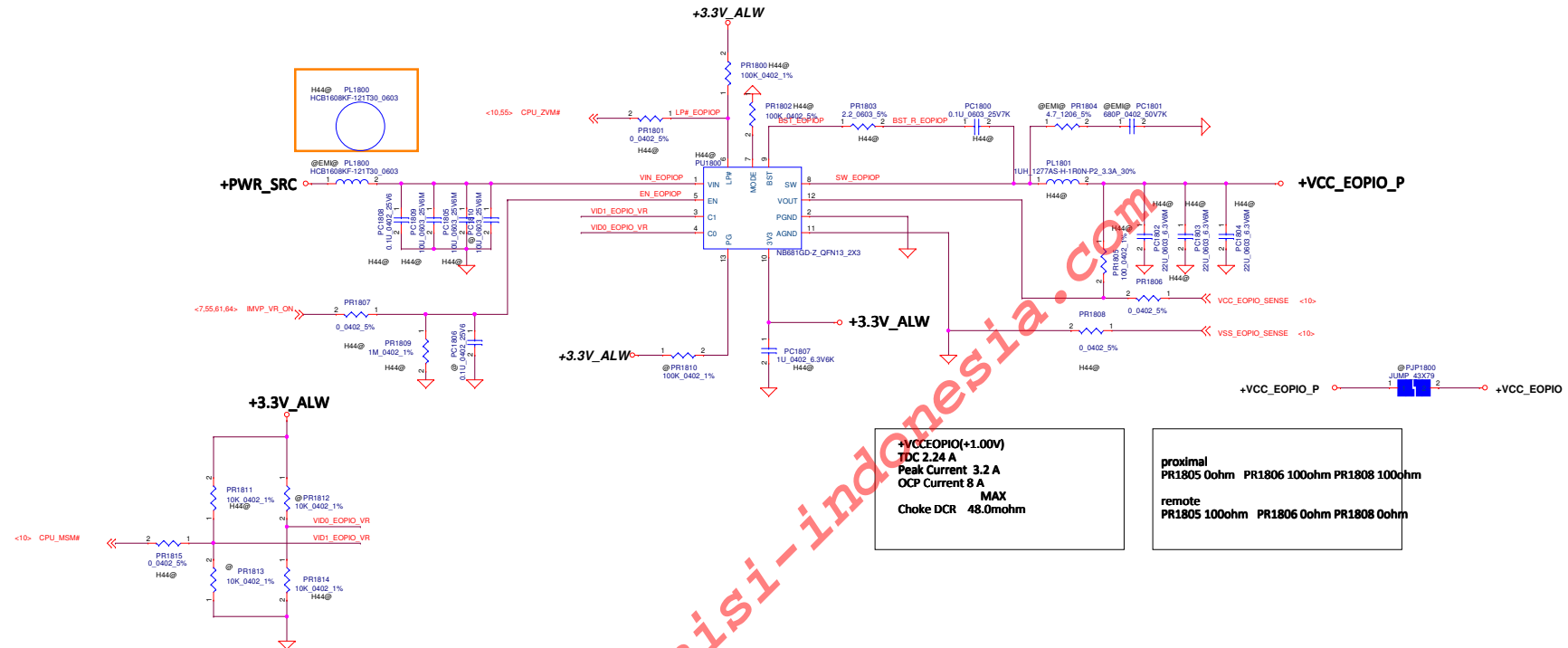
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Only H44e



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**+VCC\_EOPIO, 1V**

**LA-C551P**

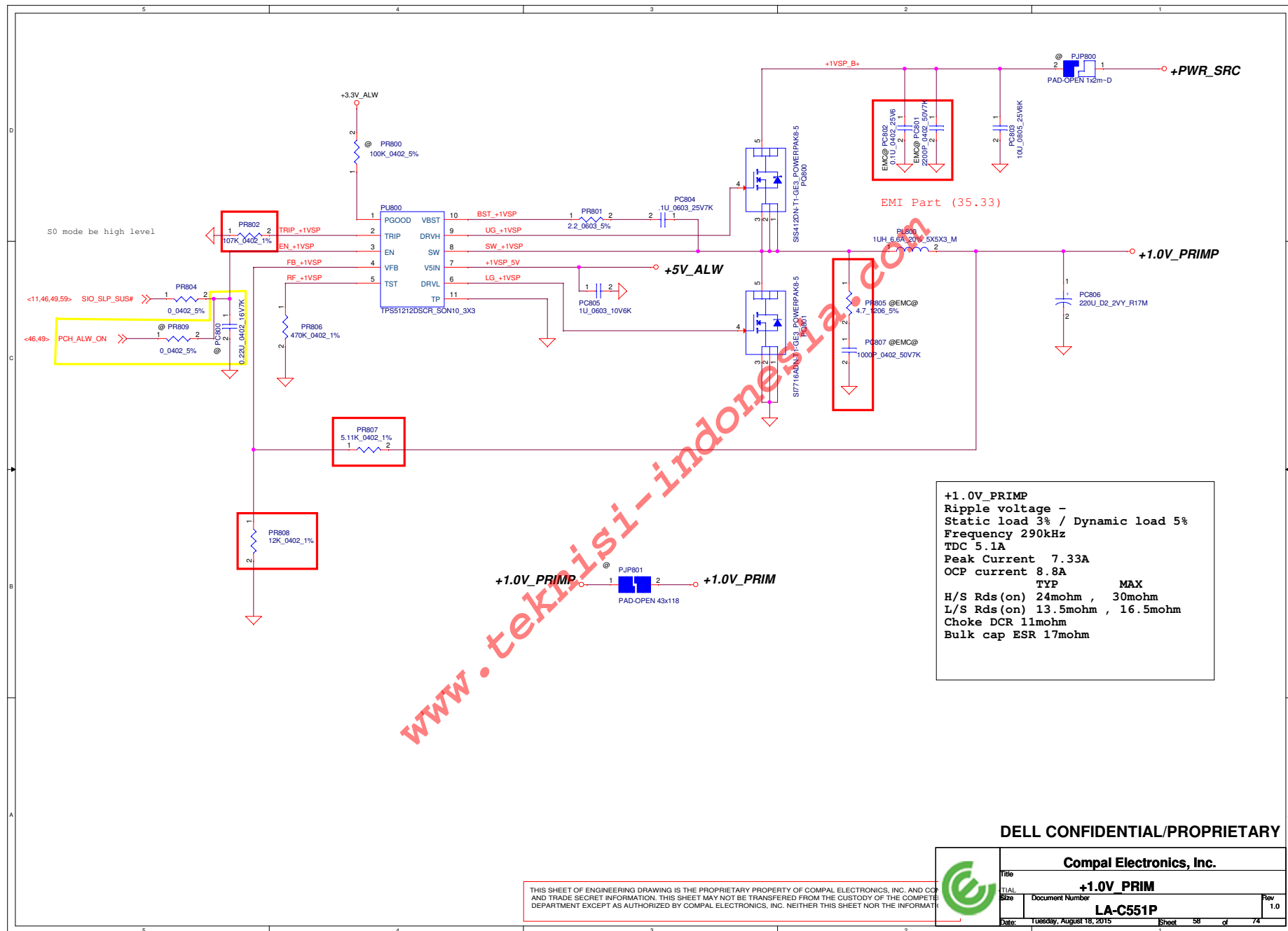
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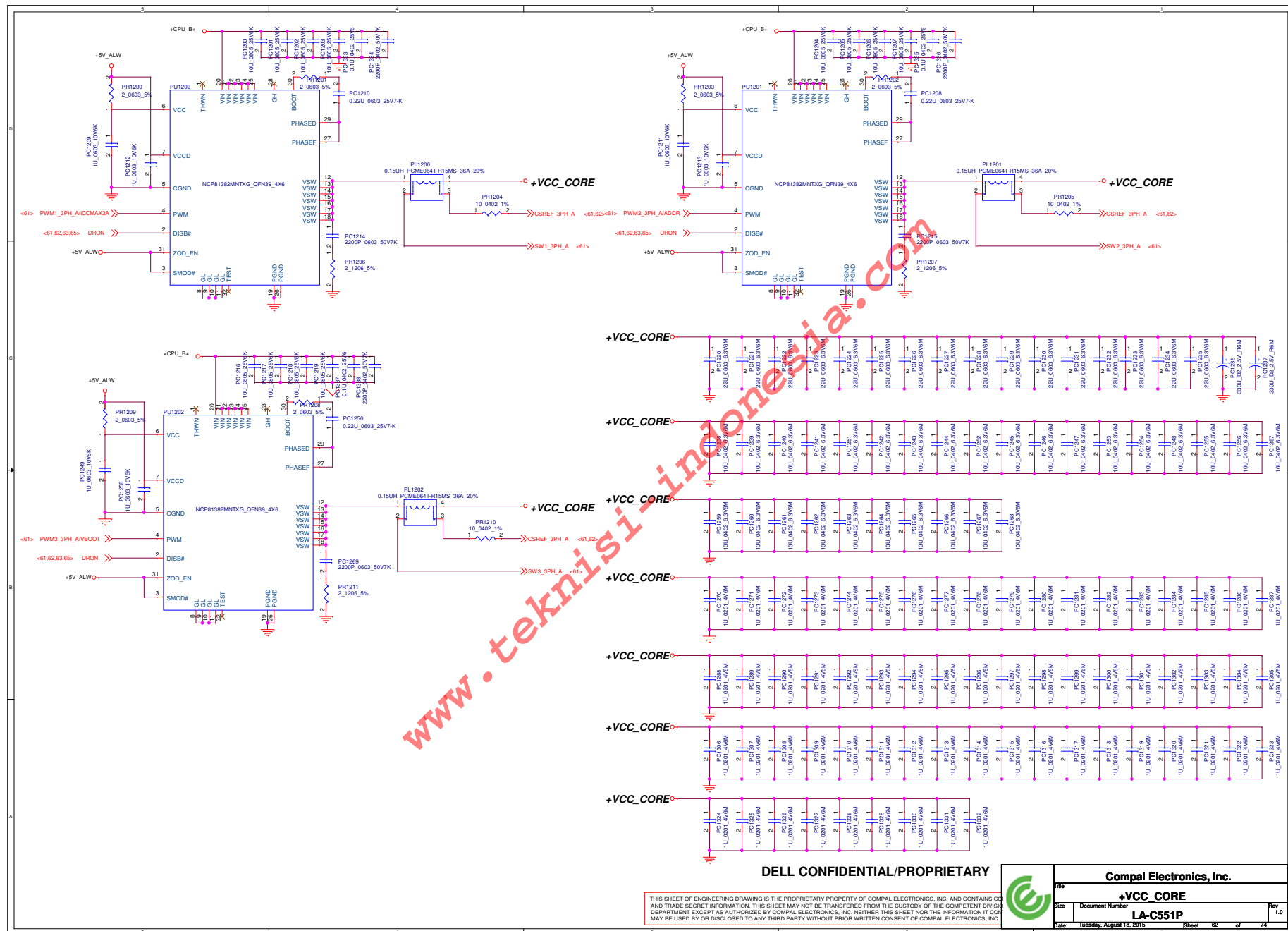


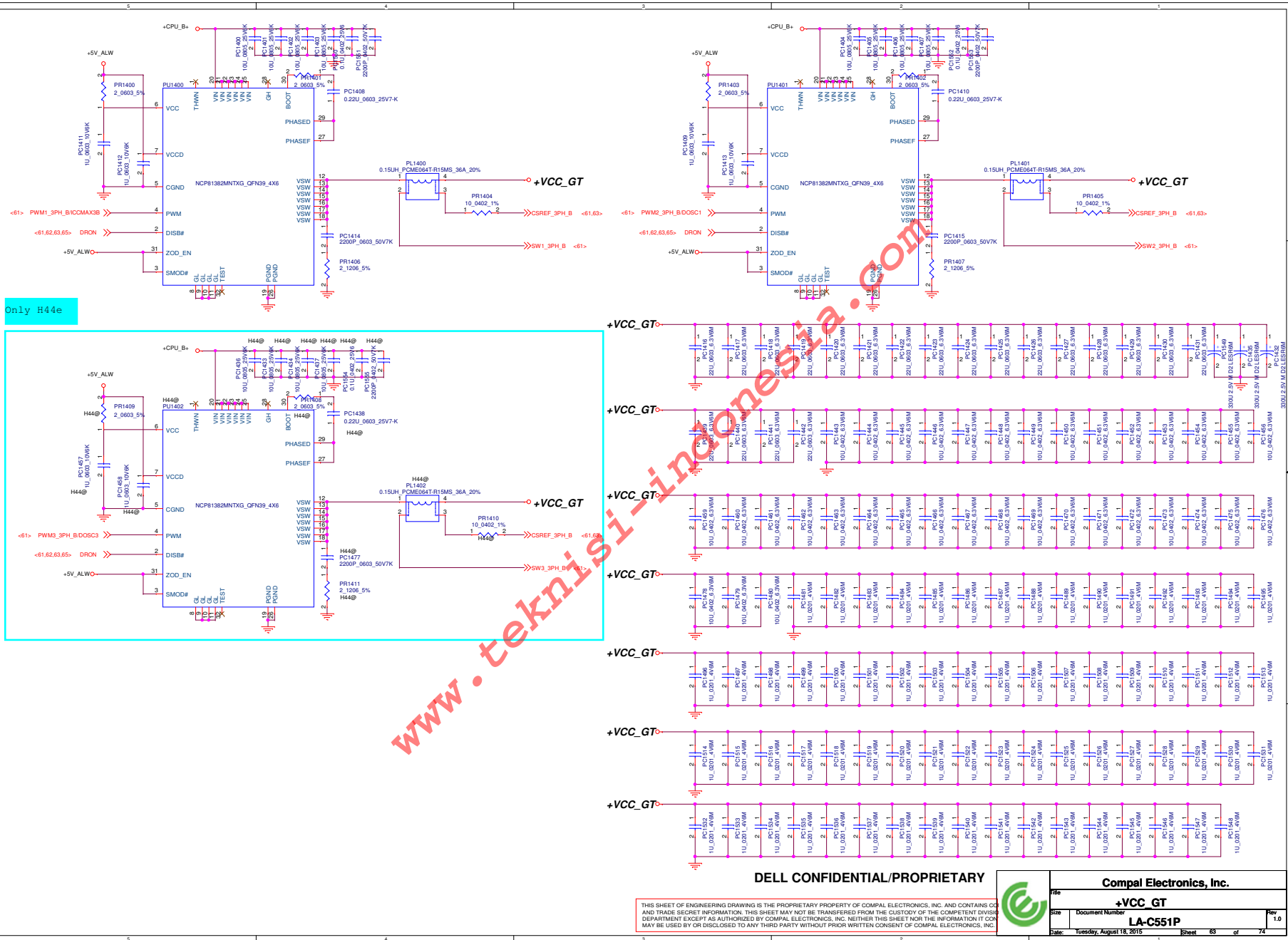












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+VCC\_GT

LA-CS51P

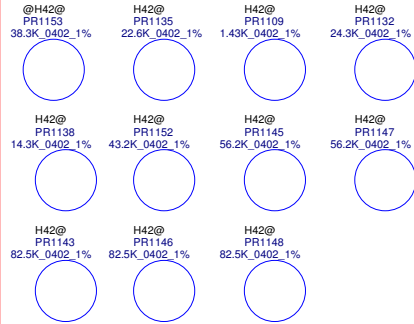
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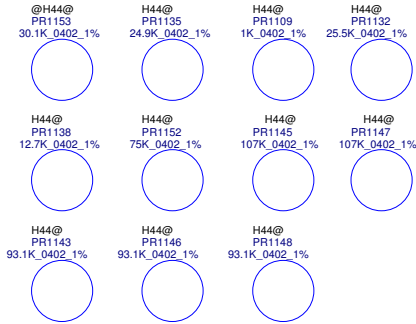




### C551\_H42 component



### C551\_H44e component



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Title		
PWR table		
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[illegible]

### Power Sequence

**D**

2015	Phase	67	0
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# Version Change List ( P. I. R.

## List)

Request Owner

Item Page# Title Date Issue Description Solution Description Rev.

1	22, 37, 49	HW	12/6/2014	compal	reserve SPI and TPM PWR rail optional +3.3V_ALW_PCH or +3.3V_M.	Add RH343,RH344,RZ75,TPM PWR rail change to +3.3V_ALW_PCH ,add @RH348 to +3.3V_M power rail option for +3.3V_1.8V_SPI.	X01(0.2)
2	37, 46	HW	12/6/2014	compal	GPIO MAP:Gen7_GPIO1211	U51.B62 change netname from POA_EN to EC_FPM_EN and U51.A9 change netname from SUS_ON to CV2_ON for follow GPIO MAP	X01(0.2)
3	45	HW	12/6/2014	compal	Avoid backdrive to +3.3V_RUN.	R3740.2(UPD_SMBUS_ALERT#) PWR rail change from +3.3V_RUN to +3.3V_ALW	X01(0.2)
4	48	HW	12/6/2014	compal	TP I2C interface reserve 0ohm	add R3752,R3758	X01(0.2)
5	28, 35	HW	12/9/2014	compal	symbol link CIS normal CPN	update U8 symbol for SA000072W00,update U31 symbol for SA000081G0L	X01(0.2)
6	24	HW	12/9/2014	AMD	avoid incorrect behavior when system w/AMD MXM cards	Reserve a pull up 10k(RH345) to +3.3V_ALW_PCH close to PCH side on GPU_EVENT#	X01(0.2)
7	25, 30	HW	12/10/2014	compal	add "+" on PWR trace netname and others no "+"	add netname +DCPRTC on CH68.1,change netname +3.3V_CAM_EN# to 3.3V_CAM_EN#	X01(0.2)
8	38	HW	12/10/2014	compal	symbol CPN and Value not match.	change C1176,C1402 PN to SGA00002B00,and depop C1402	X01(0.2)
9	30	HW	12/11/2014	compal	align BC change Q24 main source	change Q24 to SB00000QP00	X01(0.2)
10	23	HW	12/15/2014	RF	RF request	change CH268 from 0.01uF to 22pF	X01(0.2)
11	45, 46	HW	12/17/2014	compal	Gen7_GPIO1211	remove R851,R852,R853,R854,change netname CPU_ID to GPIO10,U51.A40 to MSDATA,U51.B43 to MSCLK,U51.B46 to PCH_PCIE_WAKE#,U46.A64 to ME_FW_EC,U46.A8 to USB_PWR_SHR_LFT_EN#	X01(0.2)
12	19, 42, 41	HW	12/19/2014	compal	SATA express HDD function issue-PCIE13~16 lane reverse	SATA express interface change to PCIE14(match HDD port1),PCIE13(match HDD port0),UH1.AG39 change to HDD_DET#,UH1.AD35 to SATA_EXP_IFDET.	X01(0.2)
13	46	HW	12/23/2014	compal	reserve for next-gen EC that use the Intel chipset UART TXD for the SBIOS Serouts	add R862,R863,change netname GPP_C9 to SBIOS_TX	X01(0.2)
14	46	HW	12/29/2014	compal	SB339045100 EOL	change Q28 to SB000008P00	X01(0.2)
15	22	HW	12/30/2014	compal	solve TPM PLTRST leakage	add RH346 and depop RH187,RH196, change U638.5 to 3.3V_ALW_PCH	X01(0.2)
16	6, 39, 35, 47, 22, 7, 36	HW	12/30/2014	compal	same Value a CPN on Board	PEG 0.22UF AC CAP(CC1~CC64) and SSD 0.22UF AC CAP(CN83,CN85~CN88,CN91,CN92,CN95,CN97)change from SE00000R700 to SE095224K00 U15,U58,U638,UC4 change from SA007080120 to SA007080180 Q327 change from SB00000ST00 to SB00000U000 T156 change from SP050006P00 to SP050006Y00	X01(0.2)
17	21	HW	12/30/2014	compal	DG1.0 RTC Crystal MAX ESR is 50Kohm	YH1 change to SJ10000LV00	X01(0.2)
18	42	HW	12/30/2014	compal	HDD SATA/PCIE repeater change to GEN3 chip	UN8,UN9 change from PS8555 to PS8558(SA00008DT00),CN75,CN71 change to 0.01uF,CN70,CN63,CN69,CN76,CN64,CN72,CN79,CN65,CN74,CN80,CN66,CN81 change to 0.22uF,remove CN77,CN68,CN82,CN78,add RH99~RH111,RH114~RH130	X01(0.2)
19	23	HW	12/31/2014	compal	MOW Rev1.0-To enable Direct Connect Interface (DCI),a 150K pull up resistor will need to be added to PCHHOT# pin.	RH329 change to 150kohm(SD028150380) and pop it,reserve RH347 pull up to +3.3V_RUN,add RH353,@QH5	X01(0.2)
20	37	HW	01/05/2015	compal	System will shut down as soon as system power on with FPM and RFID/NFC testing result is failed	add DZ3,RZ76,RZ72,RZ73.change JUSH1.9 from +5V_ALW2 to +5V_ALW, JUSH1.10 from +3.3V_ALW2 to +5V_ALW2,JUSH1.25 from GND to +3.3V_ALW2, JUSH1.26 from GND to +PWR_SRC.	X01(0.2)
21	39	HW	01/06/2015	compal	no business with vender-KEMET	change C619 from SGA00000N00 to SGA00002B00	X01(0.2)

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22	15, 17	HW	01/06/2015	compal	CONN LIST1124	change JDIMM2 to ADDR0106-P005A, JDIMM4 to ADDR0107-P005A	X01(0.2)
23	46	HW	01/06/2015	compal	Board ID	change R875 to 130Kohm(SD028130380)	X01(0.2)
24	28	HW	01/08/2015	compal	USH SMBUS PULL UP when wo/ USH/B	remove R3738,R3739,Q366 BS AAC@ (let them always pop w/USH or wo/USH)	X01(0.2)
25	21	HW	01/08/2015	compal	Crystal EA	change CH13,CH14 from 22pF to 15pF, C743 from 22pF to 27pF, C741P from 22pF to 33pF	X01(0.2)
26	18, 20, 30	HW	01/08/2015	compal	cost saving	change U17,UC3 from SA00003Y000 to SA000046R00,U33 from SA00003AR00 to SA00006Y800 and add @R42,change Q21 from SB000009K10 to SB000010C00	X01(0.2)
27	46	HW	01/08/2015	compal	EC5085 change CPN	change U51 to SA00006YH60	X01(0.2)
28	22	HW	01/09/2015	compal	ADD PWR net on pin16 of JSPI1	netname is +3.3V_SPI_RWR on JSPI1.16	X01(0.2)
29	22	HW	01/09/2015	compal	PLTRST group change balance before AND GATE and after	add RH349,@RH350,change RH210.1 to PCH_PLTRST#,RH337.1 to PCH_PLTRST#_AND,RH195.1 to PCH_PLTRST#	X01(0.2)
31	24	BIOS	01/13/2015	compal	AMI BIOS Bidirection debug	remove dummy net PCH_NFC_RST,add RH351,RH352 PU to +3.3V_ALW_PCH and add @RH354,@RH355 PU to +3.3V_RUN on UH1.AR39,UH1.AR45,add JUART1	X01(0.2)
32	14	HW	01/14/2015	compal	MOW rev1.0 ww02- recommended not to install any capacitor on DDR Reset signal (DRAMRST)	depop CD16	X01(0.2)
33	28	HW	01/19/2015	compal	resevrve AAC SMBUS control from PCH	add R38,R39,@R40,@R41,and R40.2 connect to UH1.AT42, R41.2 connect to UH1.AR38	X01(0.2)
34	47	ME	01/19/2015	compal	Screw hole	Add H42,H43,H44	X01(0.2)
35	10, 11	HW	01/20/2015	intel	VENDER suggestion	remove RC218,@RC219,@RC311	X01(0.2)
36	47	HW	01/20/2015	COMPAL	LED limit current R value	change R955 to 2.21k, R956 to 3k, R130 to 1.8k, R131 to 560	X01(0.2)
37	31, 32	HW	01/20/2015	COMPAL	DOCK DP1,DP2 EA	pop R119,R121 (PEQ=8.5dB) ,RV29,RV35 (PEQ=8.5dB)	X01(0.2)
38	37	HW	01/21/2015	COMPAL	TPM improve S3 support and back drive issue	Add RZ78,@RZ79,@RZ77,@RZ80,QZ2,RZ82,change U637.1 to +3.3V_ALW_PCH,U637.8 to +U637_TPM,U637.12 to NC	X01(0.2)
39	7	HW	01/26/2015	COMPAL	Solving for when system force shut down,it can't power on with power botten between 1 minute.	add @R43,@RC327,UC5,UC6	X01(0.2)
40	35	HW	03/18/2015	COMPAL	LAN EA	change L63~L70 to 0ohm(R63~R70)	X02(0.3)
41	20	HW	03/18/2015	COMPAL	546717_SKL_PCH_H_EDS_R1.2(add a 1K PD for USB2_VBUSSENSE and USB2_ID, if the signal is not used.Else it impacts Intel DCI test with warm boot)	add RH356,RH357 pull down to GND	X02(0.3)
42	43	HW	03/18/2015	COMPAL	DOCK E-SATA signal reverse	SWAP SATA_PTX_C_DRX_P1 to JDOCK1.60 (C699.1) ,SATA_PTX_C_DRX_N1 to JDOCK1.62 (C700.1)	X02(0.3)
43	37	HW	03/18/2015	COMPAL	reserve @RZ111 for modern standby,RZ112 for TPM detect issue.	add @RZ83 connect to SIO_SLP_S0#,RZ112 between PCH_SPI_CS#2_R and QZ2.2	X02(0.3)
44	46	HW	03/18/2015	COMPAL	material lack	change R374 from 0603 to 0402	X02(0.3)
45	30	HW	03/18/2015	COMPAL	for AAC function	Pop R40,R41, De-pop R38, R39	X02(0.3)
46	18	HW	03/18/2015	COMPAL	solve never detect Hot plug event input at Optimus GPU off	add R71,C1470,D95,R72change U14.1,U25.1,U27.1 from DGPU_PWROK to DGPU_PEX_RST#_D,remove @C95,@C96	X02(0.3)
47	24	HW	03/18/2015	COMPAL	reserve DIMM TYPE selection	add RC329	X02(0.3)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
48	47	HW	03/18/2015	COMPAL	material lack	change R374 from 0603 to 0403	X02 (0.3)
49	46	HW	03/18/2015	compal	Board ID	change R875 to 33Kohm	X02 (0.3)
50	47	HW	03/18/2015	compal	screw hole	Remove H15	X02 (0.3)
51	7	HW	03/18/2015	compal	XDP working	De-pop RC314,RC315,add RC330	X02 (0.3)
52	44	HW	03/18/2015	compal	Keep VBUS PWR stable	change JI02.17 from +PWR_SRC to +VBUS_DC_SS	X02 (0.3)
53	7,23	HW	03/18/2015	compal	backdrive and DG1.0	change RC315.1,RH312.1,RH314.1,RH315.1 from +1.0V_VCCSTG to +1.0V_VCCST	X02 (0.3)
54	24,30	HW	03/18/2015	compal	IR camera detect pin for verb table	add GPP_A23 to IR_CAM_DET# and connect to JEDP1 pin26,add R366 pull up to +3.3V_RUN	X02 (0.3)
55	47	HW	03/18/2015	compal	LED luminance adjust	R956 to 1k, R130 to 1k, R131 to230, R943 to 1k, R955 to 1k	X02 (0.3)
56	38	HW	04/21/2015	compal	reserve SIM detection design	add RZ113 between SIM pin1(JSIM1) to WWAN pin58(JNGFF2)	X03 (0.4)
57	48	HW	04/21/2015	compal	TP module add damping R,PU and new touchpad support PS2(in DOS),I2C bus(in OS)	Depop R3752,R3758,add RZ114,RZ115 pull up to +3.3V_TP	X03 (0.4)
58	45	HW	04/24/2015	compal	BITS211484: Left IO/B USB port 1 can't charge smart mobile device under S3/S4/S5	add RE72,RE73,RE74,RE75,RE76 pull up to +3.3V_ALW.	X03 (0.4)
59	45	HW	04/27/2015	DELL	AAC update BOM for mic	change C1420 and C365 from 0.1uf to 2.2uF.	X03 (0.4)
60	28	HW	04/27/2015	broadcom	USH reset by BCM58102	depop RH359	X03 (0.4)
61	18	HW	05/18/2015	NVIDIA	add test pad on DVI_HPD of MXM	Add T217 on DVI_HPD	X03 (0.4)
62	46	HW	05/18/2015	NVIDIA	common EC code	change U51 from SA00006YH60 to SA00006YH30.	X03 (0.4)
63	47	HW	05/18/2015	compal	HDD active LED behavior for PCIe M.2 SSD module	add D97,D98,D99,and add R383 PU to +3.3V_RUN,R384 PU to+3.3V_SSD1, R385 PU to +3.3V_SSD2	X03 (0.4)
63	48	HW	05/21/2015	compal	BOM change for Touchpad function	pop CZ30,CZ31 and change them to 330pF	X03 (0.4)
63	44,45	PWR	05/21/2015	compal	TBT PD power support	change JI01.36 from GND to DCIN_ACOK#,and add PROCHOT_GATE on U46.A61	X03 (0.4)
64	45	BIOS	05/21/2015	compal	EC detect for AR/B or non AR/B	change JI01.34 from GND to PD_ACE_DET#,and add it on U46.A60 and RE77 PU to +3.3V_ALW	X03 (0.4)
65	46	HW	05/22/2015	compal	board ID	change R875 from 33Kohm to 4.3Kohm	X03 (0.4)
66	41,47	HW	05/22/2016	compal	HDD active LED behavior for SATA EXPRESS HDD	add U639,R386,D100,and add R387 PU to +3.3V_RUN	X03 (0.4)
67	26	HW	05/22/2016	compal	reserve 0.1uF for 5.76G noise	add @CH269	X03 (0.4)
68	44	HW	06/15/2016	compal	GPIO pin can direct PU/PD no need serise R to limilt current	change R388 from 10kohm to 0ohm	X04 (0.5)
68	44	HW	06/15/2016	compal	QS CPU no need PD on SPI0_IO3 for boot	depop RH334	X04 (0.5)

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69	18	HW	06/15/2016	compal	MXM3.1 SPEC	remove @R6,@R1979,change JMXM1 pin268,pin270 to +3.3V_MXM	X04(0.5)
70	19, 45	HW	06/15/2016	compal	reserve GPIO pin for tell EC don't read GFX Temp.in GC6	connect RH342.1 to U46.A48,remove R3749	X04(0.5)
71	45	HW	06/15/2016	compal	PROCHOT_GATE initial status	add @R415 PU to +3.3V_ALW,R416 PD to GND	X04(0.5)
72	46	HW	07/05/2015	compal	power on/off sequence tCPU05/tPLT18/tCPU03 and global reset issue	add U9,@C787 for tCPU05 and tPLT18,add RC331,CC273 for tCPU03,add @Q370,R435 for global reset	X05(0.6)
73	37	HW	07/05/2015	compal	TPM DS3 support	change U637.1 from +3.3V_ALW_PCH to +3.3V_ALW	X05(0.6)
74	46	HW	07/05/2015	compal	Board ID	change R875 from 2kohm to 1kohm	X05(0.6)
75	42	HW	07/29/2015	compal	SATA IEMT CTLE(change RX EQ from level 1 to 2)	pop RN130	A00(1.0)
76	41	HW	07/29/2015	compal	SATA PWR supply for over loading	pop C404,change C403 for 0.1uF to 22uF,and pop it.	A00(1.0)
77	11	HW	07/31/2015	compal	VCCPLL_OC power gate requirement for Deep Sleep support	depop RC302,add UZ30,@RC330,@CZ95,@CZ96,CZ97,UC7,@CZ98	A00(1.0)
78	7, 23	HW	08/07/2015	compal	backdrive and CPU EDS0.95	change RC135.1,RH312.1,RH314.1,RH315.1 from +1.0V_VCCST to +1.0V_VCCSTG	A00(1.0)
79	46	HW	08/03/2015	compal	Board ID	change R875 from 1kohm to 62kohm	A00(1.0)
80	22, 35, 46	HW	08/07/2015	compal	MP component CPN	change UH1 to SA00009602L,U31 to SA000081G1L,U51 to SA00006YH90	A00(1.0)
81	7, 23, 28, 44, 49	HW	08/13/2015	compal	MP BOM change	depop R3739,R3738,R40,R41,U8,C31~C36,R23~R30,C141,C143,C365,C1420,R373,R375,R414,R410,R413,R411,R361,R362(drop AAC),SW1,SW2,R3728,UZ28,C513,C547,pop RC301	A00(1.0)
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1	P57	POWER	1/6	COMPAL	BQ24780 IFAULT LOW latch off	1. PC702 chagne to 0.1uF 2. PC704 change to 0.01uF	PR02
2	P51	POWER	1/6	COMPAL	PU101 change to TPS51285B	1. PU101 change to TPS51285B 2. PC100/PC118 chagne to 4.7uF 3. add PR114 4. PR105 change to 29.4k ohm 5. PR106 change to 31.6k ohm	PR02
3	P64	POWER	1/19	COMPAL	VCC_GTU sense	Add PR1620/PR1621 100ohm	PR02
4	P61	POWER	1/28	COMPAL	VCORE parameter adjust for vendor request	1. PR1109 change to 1.43k ohm 2. PR1137/PR1133 change to 3.65k ohm 3. PC1121/PC1124 change to 100pF 4. PR1132 change to 25.5k ohm 5. PC1123/PC1125 change to 0.1uF 6. PC1104 change to 2200pF 7. PR1112 change to 30k ohm 8. PC1107 change to 6800pF 9. PR1135 change to 24.9k ohm 10. PR1152 change to 75k ohm	PR02
5	P52	POWER	3/18	COMPAL	change unmount for HW request(power sequence)	PC215 change to numount	PR03
6	P53	POWER	3/18	COMPAL	Add RC for HW request(Power sequence)	Add PR317/PC312	PR03
7	P57	POWER	3/18	COMPAL	change to connect RENG for BATTERY reverse input protection	Add PD703 in IC RENG pin	PR03
8	P64	POWER	3/18	COMPAL	change VCC_GTU parameter for Vendor request	PR1604 change to 6.19k ohm add PC1690 to 4700p F	PR03
9	P57 P60	POWER	3/24	COMPAL	Add circuit to prevent +SDC_IN oscillation	Add PD704/PR766~PR770/PQ708 Add PD1101/1033~PR1037/PQ1005	PR03

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10	P61	POWER	3/26	COMPAL		Add PR1170 for CPU H LINE-42	Add PR1170	PR03
11	P57	POWER	4/29	COMPAL		change CHARGER parameter for Vendor request	PR744 change to 37.4k ohm	PR03
12	P57	POWER	4/30	COMPAL		Add circuit to detect type C current	Add PQ1073(SB000000DH00) /PR771(SD028000080) ,PR772(SD034100380) ,PR773(SD028000080)	PR04
13	P61	POWER	4/30	COMPAL		change VCORE parameter for Vendor request	PR1153 change to 30.1k ohm(H44e) 38.3kohm(H42)	PR04
14	P60	POWER	5/8	COMPAL		Add circuit for avoiding type C current to flow to battery	Add PD1102/PD1103(SCS0340L010) /PR1026 100ohm(SD014100080)	PR04
15	P57	POWER	5/14	COMPAL		Change the charger ILLM circuit for current sense	PR758 from 18K to 20K ,PR760 from 3.16K to 5.36K and PR764 from 20K to 2.74K	PR04
16	P57	POWER	5/19	COMPAL		Add circuit for the PD	Add PC151(SE102104K00) / PQ1074(SB000000DH00) / PU105(SA007080120)	PR04
17	P50	POWER	6/8	COMPAL		Add diodes for ESD team request	Add PD4/PD6(SCA000000T00)	PR05
18	P50	POWER	6/15	COMPAL		Change PU1 for ESD issue	Change PU1 from SA00003DN00 to SA00001WK00/ depop PD4/PD6	PR05
19	P61	POWER	6/23	COMPAL		change VCORE parameter for IPCC solution	PR1153 change to 24.9k ohm(SD034249280)	PR05
20	P52 P53	POWER	7/6	COMPAL		For tCPU05 (VDDQ 1.2V to VCCIO 1.0V) add one AGATE 7408 and control by SIO_SLP_S3# and 1.2V_SUS_PWRGD(for HW )	Depop PC312/PR303 Remove PR317 Change EC netname(to HW) from SIO_SLP_S3# to RUN_ON_AND Pop PR209 Add offpagethe for 1.2V_SUS_PWRGD	PR06

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